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Filter using fast binary counters based on symmetric stacking

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Abstract: Multipliers are significant in the present computerized signal preparing and different applications. With advance in innovation, numerous explores have attempted and still are attempting to structure multipliers that offer both of the accompanying plan targets rapid, low force utilization, consistency of design and subsequently less region or even a mixed combination of these in one single multiplier along these lines that makes them appropriate for different speed, low force along with reduced VLSI usage. In existing Wallace multipliers are utilized to ascertain fractional items and full adders are utilized as counters which utilizes no XOR doors. To diminish deferral and force utilization full adders and half adders are supplanted with bit stacking. A basic low force fir channel is structured utilizing stacking idea.

Keywords: Filter, multiplier, counter, stacking, adder

1. INTRODUCTION

To join half-way items proficiently, section pressure is ordinarily utilized in multiplier circuits. Numerous strategies have been introduced to streamline the presentation of half-way item summation, for example, notable line pressure methods in "***Wallace tree or Dadda tree"***, or the other enhanced. These kinds of strategies include utilizing full adders filling in as counters to be enhanced. This kind of strategies include utilizing full adders filling in as counters to lessen gathering of 3 bits of a similar load in equal utilizing of convey spare viper tree. Through a few layers of decrease, the quantity of summands is diminished to two, which are then included utilizing an ordinary snake circuit. The 6:3 and 7:3 counters are acknowledged by first stacking the entirety of the information bits to such an extent where the assembled ones are entirety of the "1" bit. In the wake of stacking the info bits, it is possible to change the stack over into a parallel tally to yield the 6-piece check. In order to shape 3-piece stacks, firstly the little 3-piece stacking circuits are utilized. Further, the mentioned 3-piece stacks are then merged in order to make a 6-piece stack utilizing a particular procedure which contains one additional layer of rationale.

X0, X1, and X2 are the given sources for information. There is a 3-piece stacker circuit having Y0, Y1, and Y2 as 3 yields to a particular extent where the amount of "1" a bit in the yields is actually like the amount of "1" bits in the data sources. Though, to the one side "1" bits are gathered followed by the "0" bits. Further the yields were actually shaped without any mistake by

$$Y0 = X0 + X1 + X2,$$

$$Y1 = X0\ X1 + X0\ X2 + X1\ X2,$$

$$Y2 = X0\ X1\ X2$$

Especially, here principal return is "1" in case any of the information sources is one, "1" will be the subsequent return in case any two of the sources for data are one, and further, the last yield will be one in case of all the three sources of information are "1." Here Y1 return is a uttermost work, which is achieved by using one mosaic CMOS door Fig.1.1. Below represents the 3-piece stacking circuit:

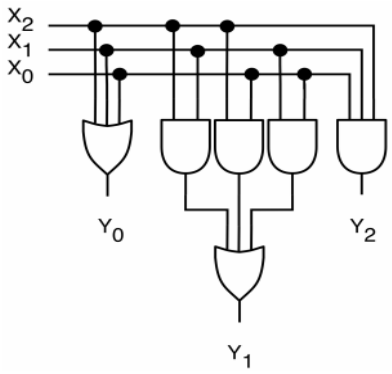

Figure1.1: 3-bit stacking circuit

Counters are utilized to check the quantity of ones from the given info. In the current work 6:3 and 7:3 counters are utilized. Those 6:3 and 7:3 counters comprised of full adders as well as the half adders are talked about beneath. Lessen gathering of 3 bits of a similar load in equal utilizing of convey spare viper tree. In order to combine the partial products efficiently, column compression is commonly used in Multiplier circuits. Numerous strategies have been introduced to advance the presentation of the fractional item summation, for example, the notable line pressure procedures in the Wallace tree or Dadda tree, or the other improved structures. These techniques include utilizing full adders working as counters to lessen gatherings of 3 bits of a similar load to 2 bits of various load in equal utilizing a convey spare snake tree. Through a few layers of decrease, the quantity of summands is diminished to two, which are then included utilizing a regular snake circuit.

2. 7:3 AND 6:3 COUNTERS USING FULL AND HALF ADDERS:

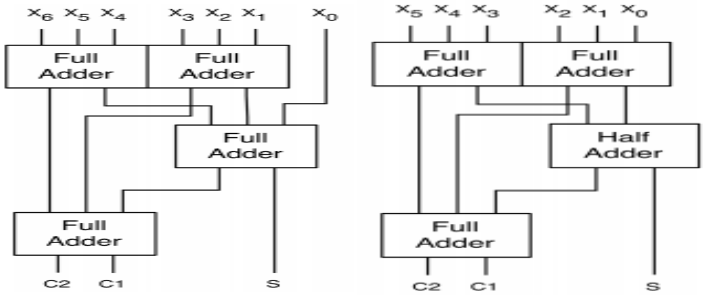

Fig2.1: 7:3 and 6:3 Counters using Full and Half adders

The current Wallace multiplier contains counters that are comprised of full adders as well as half adders. The 6:3 and 7:3 counters worked with full adders are appeared in Fig.2.1. Here X shows the contributions for both the 6:3 and 7:3 counters. Each full viper takes three sources of info and gives two yields as total and convey. The viper yields are given as C1, C2 and S. At long last, these counters include the quantity of ones in the given info.

2.1.1 Example for 7:3 using full adders:

Model for 7:3 counters utilizing full adders is appeared in the Fig.2.1.1. Here, inputs X6, X5, X4, X3, X2, X1, X0 = 1 0 1 . Each full adders have three information sources which gives aggregate and convey as yields. At that point all the total yields are again given to another full viper alongside X0. Remaining convey yields are given to another full snake. At that point the snake yields are given as C1, C2 and S. As the quantity of one's given = 6, at that point we get yield of the viper as 1 0 i.e., in parallel arrangement.

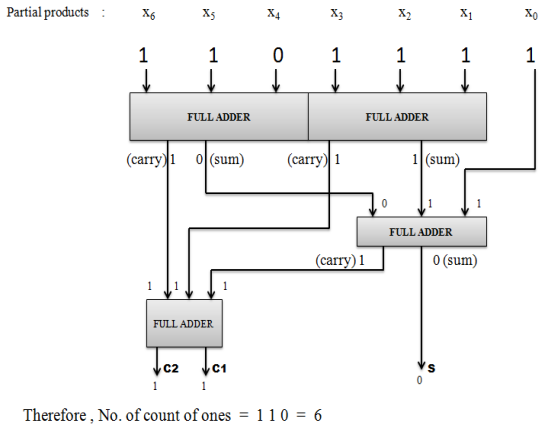

Fig2.1.1: Example for7:3 Counters using Full adders

2.2 Example for 6:3 using full adders and half adders:

Model for 7:3 counters utilizing full adders is appeared in the Fig.2.2.1. Here, inputs X6, X5, X4, X3, X2, X1, X0 = 1 0 1 . Each full adders have three information sources which gives aggregate and convey as yields. At that point all the total yields are again given to another full viper alongside X0. Remaining convey yields are given to another full snake. At that point the snake yields are given as C1, C2 and S. As the quantity of one's given = 6, at that point we get yield of the viper as 1 0 i.e., in parallel arrangement.

For the most part Wallace fast multipliers utilize full adders and half adders in their decrease stage. But half adders do not reduce the number of partial bits. This conventional method that is multiplier with half adders and full adders is modified in such a way that left half of the array is shifted upwards i.e., pyramid structure. The reduction stages in this modification remains same but it utilizes whatever number full adders as could be expected under the circumstances however distinction is it possibly utilizes half adders when important. Changed Wallace decrease technique partitions the network into three gatherings and uses full adders for each gathering of three bits in a segment. Single bits are passed to next stage.

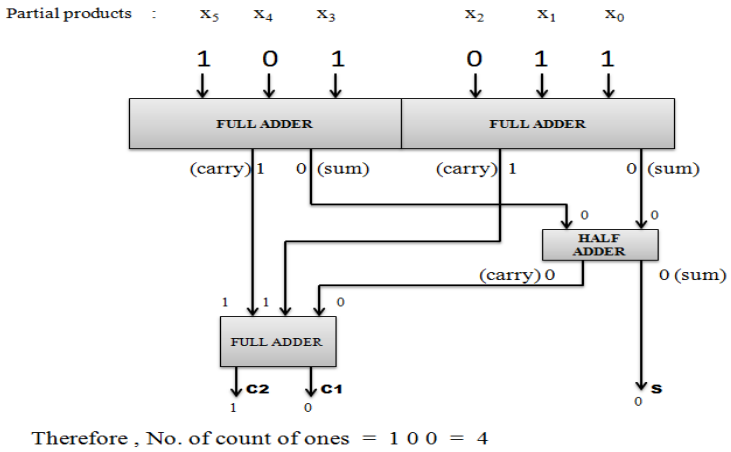

Fig.2.2.1 Example for 6:3 counters using full and half adders

2.3 Conventional Wallace multiplier:

As shown in the figure, explosion is used to address the half-way objects in case of Wallace multiplier. Right of most section is known as Segment 0. Counters used in each section are spoken to by the crates around the dab items. The case in question speaks to 3:2 and 2:2 counters. Here, the stages are leveled with level's dark separation line. Fractional items are reduced at each stage. Finally, it was added to obtain the last one item. Dab outline of 16x16 customary multiplier is represented in below Fig.2.3.1.

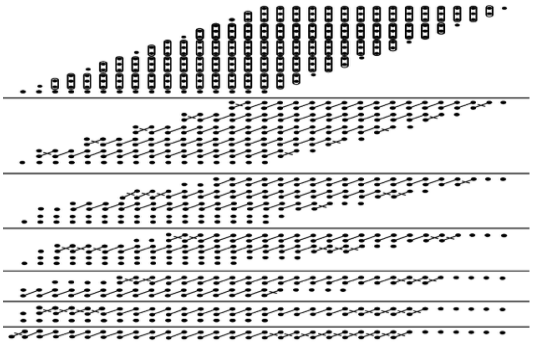

Fig.2.3.1: Conventional Wallace Multiplier

3. FIR FILTER USING FAST BINARY COUNTERS BASED ON WALLACE MULTIPLIER:

3.1 Introduction:

The Wallace multiplier utilizing stacking idea is utilized in FIR (Finite Impulse Response) channel. Right off the bat, a MAC unit is planned and later this unit is utilized to structure FIR channel. A low pass FIR channel is structured utilizing MATLAB program. This program is used to generate the coefficients. Later these coefficients are used to generate low pass FIR filter using Wallace multiplier.

3.2 MAC unit design:

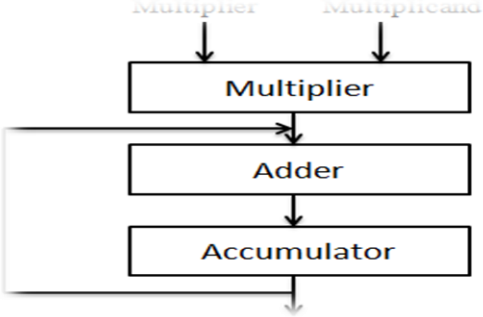

Fig.3.2.0: MAC Unit Design

In almost all the applications of DSP, there is a requirement of the computation of the sum of the products of a series of succeeding multiplications. MAC known as a “multiply and Accumulate unit” is a special unit which is used to implement such kind of functions. There are two components in a MAC that is a multiplier and a particular register called Accumulator. To implement functions like A+BC, MACs are being used and the figure3.2.0 below shows a typical MAC unit.

3.2.1 Counter Based Wallace (CBW) Multiplier:

The spot documentation is utilized to speak to the fractional results of the CBW multiplier talked about in this area as appeared in Figure3.2.1. Here right most sections is called segment 0. The counters in every section are spoken to by the crates around the dab items. Box encasing seven, six, five, four, three, and two spots speaks to 7:3, 6:3, 5:3, 4:3, 3:2, and 2:2 counters, separately. The stages are isolated by a thick flat line. The engineering of CBW multiplier depends on the keen utilization of rapid counters.

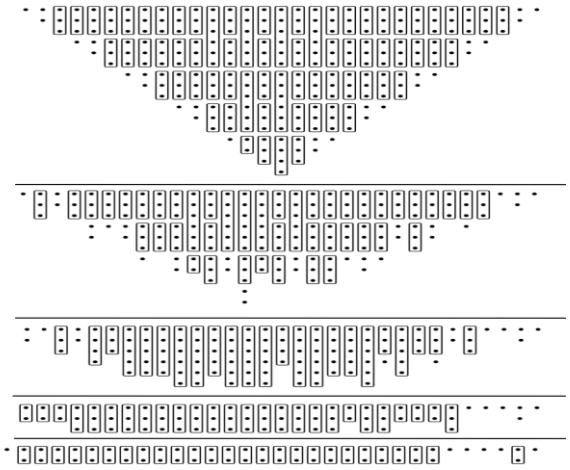

Fig.3.2.1 Counter Based Wallace Multiplier

3.2.2 Example for MAC unit design:

Here 'a' (16-bit) and 'b' (16-bit) are multiplier and multiplicand. Both 'a' and 'b' are multiplied using Wallace Multiplier which is designed by symmetric stacking method using 6:3 counters. After, multiplication product (m1) is obtained. Accumulator adds the product (m1) and the given feedback (C) which gives the final output.

4. FIR unit design:

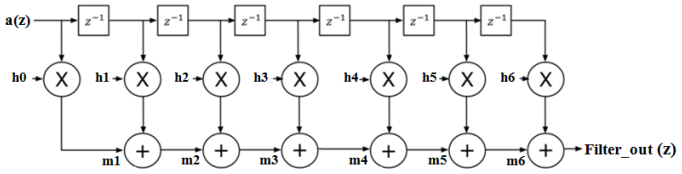

Fig.4.0: Linear Phase Structure of Low Pass FIR filter Design

In signal processing, a particular filter which has impulse response of a finite duration or output to any input of a particular measurable length is "**Finite Impulse Response (FIR)"** filter as in a finite time it settles to Zero. This is in compare to "**infinite impulse response (IIR**)" filters, that can have feedback internally which also may continue to retort indirectly (ordinarily decreasing). A seven tap low pass finite impulse response is shown in fig.4.0. Here **a(z)** is input and **filter out (z)** is output and b0, b1, b2, b3 are coefficients. Input values a (z) are multiplied with coefficients "h0, h1, h2, h3, h4, h5, h6". Similar to MAC these product values are added to the feedbacks which are represented as m1, m2, m3, m4, m5, m6. And finally output is given as filter out (z).

4.1Generation of FIR filter coefficients:

A low pass FIR filter is implemented using MATLAB programming. First a LPF is designed by usage of rectangular window by taking 7 samples of window sequence with a cutoff frequency of 0.2π radians per sample. The program for LPF by usage of rectangular window is shown below:

```
close all;
clear all
wc=.2*pi;
N=7;
t=(N-1)/2;
eps=.001;
n=0:1:N-1;
hd=sin(wc*(n-t+eps))./(pi*(n-t+eps));
winr=boxcar(N);
hn=hd.*winr'
w=0:.01:pi;
h=freqz(hn,1,w);
subplot(2,2,1);
plot(w/pi,(20*log10(abs(h))));
title('rectangular window');
ylabel('gain in dB');
xlabel('normailsed frequency');
subplot(2,2,3);
plot(w/pi,angle(h));
ylabel('phase');
xlabel('normalised frequency');
```

Fig.4.1.1: LPF MATLAB program utilizing rectangular window

The coefficients generated using rectangular window for low pass FIR filter by taking 7 samples are represented with **hn** which are shown in fig 4.1.1. To convert floating-point to fixed point number the generated FIR filter coefficients are multiplied with ((2^15) - 1) i.e., with 32767. As, a 16 bit Wallace multiplier is used in FIR filter numbers to be no larger than 32767. Therefore, the coefficients are changed to fixed point format which are shown in below figure.4.1.2.

```
>> firlpf

hn =

    0.1010    0.1514    0.1871    0.2000    0.1871    0.1513    0.1009

>> hn*32767

ans =

   1.0e+03 *

    3.3083    4.9613    6.1315    6.5534    6.1298    4.9583    3.3047
```

Fig.4.1.2: Low Pass FIR filter Coefficients

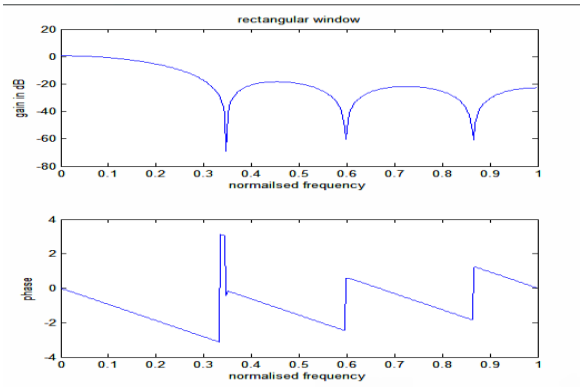

Fig.4.1.3: Low Pass Finite impulse response filter Phase and Gain characteristics

5. CONCLUSION:

A symmetric stacking-based Wallace Multiplier is used in Low Pass FIR filter for multiplication to obtain a product efficiently i.e., with low delay and less power consumption. When compared to normal FIR filter which uses normal multiplication this FIR filter has decreased the delay and power consumption up to 61 percent and 5.95% respectively.

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