

# Design of low power full adder using MGD I logic

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**Abstract:** Full adder is an essential component to design different digital systems and it is used in wide applications like microprocessor and microcontroller and also digital signal processors. There is a high command in electronic devices and circuits, and then it requires low power and high speed. Here, the present paper illustrates the significance of power, delay and a transistor count. The investigation and outline of 8TMGDI full adder style is observed. This full adder is maintaining some low power complexity. The presentation and application of the modified gate diffusion full adder are compared to other full adders like CMOS and GDI. The simulation results of the 8T modified gate diffusion full adder shown better power and delay values, when compared to the other full adders. This paper gives the best results in the low power technology. In 45nm Technology virtuoso tool, the proposed full adder is designed and compared.

**Keywords:** Gate Diffusion Input logic, Modified Gate Diffusion Input logic, Full adder circuit, CMOS logic.

## 1. Introduction:

In the most arithmetic components, binary addition is only the fundamental operation. At low power consumption and a high speed, area systematic designs have needed arithmetical calculations. The recognizing of full adders is a significance of high performance and low power. The importance of expanding the presentation of a system is to appear the presentation of full adders. In low power applications, full adder designs are places a major role [1].

Some applications are there in VLSI. They are nothing but battery power and fast growing mechanics in communications. The VLSI design structure is look like as lofty in command because its applications. However, gate diffusion technique is the well organized method in the low power design technique. In high speed data communication structure, multiplexer executes an important role in VLSI. A multiplexer is used productively in the number of implementations as well as network switches, digital signal processors and processors. The features of the mechanization are compared to average power and delay. The objective of the present full adder circuits is to reduce the speed power, and delay. This 8T modified gate diffusion input full adder is compared to the 14T MVT-GDI full adder, 10T GDI full adder and also 16T hybrid full adder. Transistor count and power are some of the main features in this paper.

### 1.1 GDI technique:

Gate diffusion input is only the best well-liked method in modern times. The Gate diffusion input method is managed with two transistors to design logic gates. The logic gates are nothing but OR, AND, NOR, and MUX. The formation of GDI cell is as shown in figure 1. The Gate diffusion input structure is as same as inverter but functionality is different. GDI cell carries three inputs. They are:

1. G - it is input to the both Nmos transistor and Pmos transistor.
2. P - it is input to the Pmos transistor.
3. N - it is input to the Nmos transistor.

Firstly, the GDI method was initiated the fabrication process in both twin-well CMOS processes and silicon on insulator. GDI has the power to design the logic gates with two transistors.

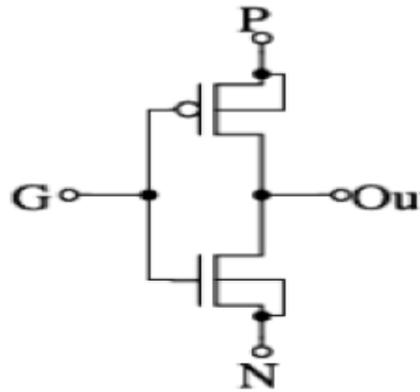


Figure. 1. basic gate diffusion input cell.

### 1.2 Modified gate diffusion input technique:

In low power digital circuits, modified gate diffusion input is also the new method in VLSI. This method is embraced from the gate diffusion input method. MGDI is used to decrease average power, transistor count, and also other parameters like delay. One of the main points in MGDI technique is to improve the design or circuit presentation and consume some information from GDI technique. The benefits of MGDI technique is to keep down the spending of total power and the transistor count. P, N, and G are the three input terminals of the modified gate diffusion input design. The formation of modified gate diffusion input is shown in the figure 2. In that place, some drawbacks of gate diffusion input logic are there. MGDI overcomes the drawbacks with the influence of the source body and technology scaling.

The bulk junction of the pmos transistor is attached to supply. The bulk junction of the nmos transistor is attached to ground. By using the CMOS fabrication process, MGDI design is also executed.

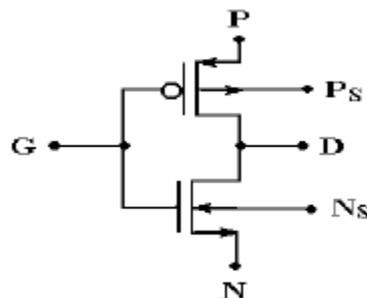


Figure. 2. basic modified gate diffusion input cell.

## 2. Brief views of existing full adders:

### 2.1 Cmos full adder:

In VLSI, only the most conventional approach design is Static Complementary Metal-Oxide-Semiconductor full adder. The CMOS outline is mainly comprises of 28 transistors. The CMOS design is mainly consists of pull-up or p-mos transistors and pull-down or n-mos transistors [3]. Voltage scaling and transistor sizing are the advantages of CMOS design. CMOS design is supplies full swing logic, it is very important to design the compound structures. One of the drawbacks in CMOS design circuits are very high input capacitance, and also further area in its structure. In terms of power consumption and transistor count static CMOS full adder design is alike the mirror adder. The Mirror adder is one of the dressed designs in VLSI.

### 2.2 10T GDI Full adder:

In this 10T GDI full adder, 4 clarified GDI full adders are suggested. The advantages of this 10T GDI full adder design are high flexibility and less transistor count. It can be perceived using quality of the p-well procedure [5]. The 10T GDI full adder is tolerate from poor driving capability [9].

### 2.3 16T Hybrid full adder:

16T hybrid full adder circuit design is utilizing both the transmission gate logic and CMOS logic announced [7]. 16T hybrid full adder design is executed for 1-bit and then expanded to the 32-bit also. This design is executed in cadence tools 90 and 45 nanometre technology. The limitations like average power, delay and the transistor count are differentiated with more full adder designs. The disadvantages of this 16T hybrid full adder design are low speed, so we go for other full adder designs.

### 2.4 14T MVT-GDI Hybrid Full adder:

14T MVT-GDI full adder which utilizes both MVT and GDI. In this design, 14 transistors are presented [10]. In cadence-virtuoso tools, the 14T MVT-GDI full adder is executed in 45 and 90 nanometre technologies. The present 1-bit full adder is compared to all other full adders. The advantage of the ultra-low voltage operation is obtaining and reaching minimum energy consumption.

### 3. Design of the proposed full adder circuit:

8T MGDI full adder circuit design is mainly consists of 8 transistors with modified technique. Sum and carry are the two expressions of the 8T MGDI full adder. The proposed full adder circuit has its low power and it contains lesser transistors when differentiated to the 10T gate diffusion full adder, the 16T hybrid full adder, the CMOS full adder. This is the best technique in low power applications. The benefits of 8T MGDI design are its speed. The operation of this full adder contains three inputs those are nothing but A, B, C and two outputs those are nothing but SUM and CARRY.

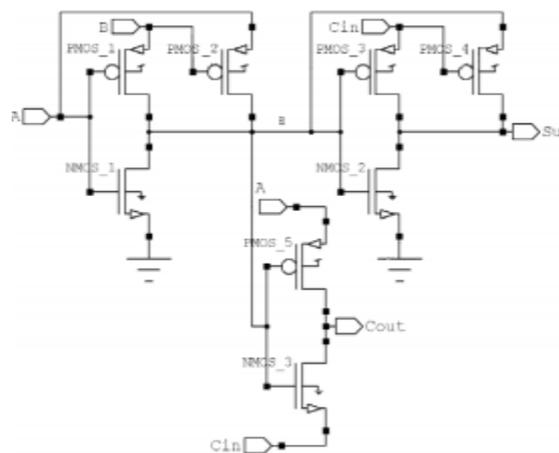


Figure. 3. 8T MGDI full adder

The schematic sketch of the 8T MGDI full adder is as shown in the figure. 4. The above circuit is designed with the help of p and n-mos transistors and also ports like input pin, output pin, supply and ground. MGDI is different from other techniques. At the output stage of GDI technique, it is not feasible to get a strong 1 and strong 0. To control these disadvantages of GDI-cell, it is better to search for other new modified techniques. The bulk end is not suitably biased, and this circuit shows threshold drop. This is the main disadvantage of relation with GDI. MGDI is relevant for designing low power circuits, high speed with lesser number of transistors. The benefits of MGDI design is to enhance the swing restoration. By using the small cell library, it allows top-down design.

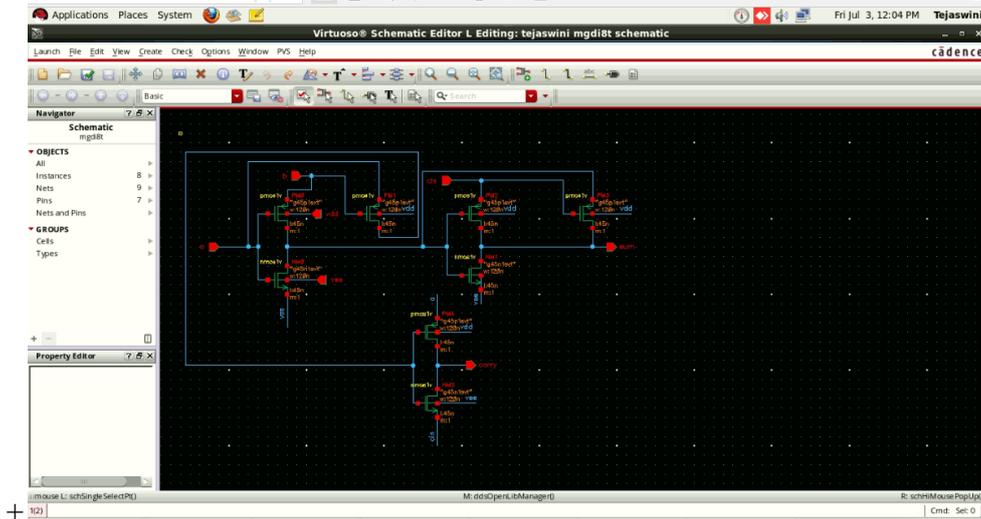


Figure. 4. schematic of 8T MGDGI full adder

#### 4. Results:

The simulation of 8T modified gate diffusion input full adder is as appeared in fig.5. This waveform gives the best results. Average power and delay is calculated by using this waveform only. Transistor count also considered with the help of waveform.

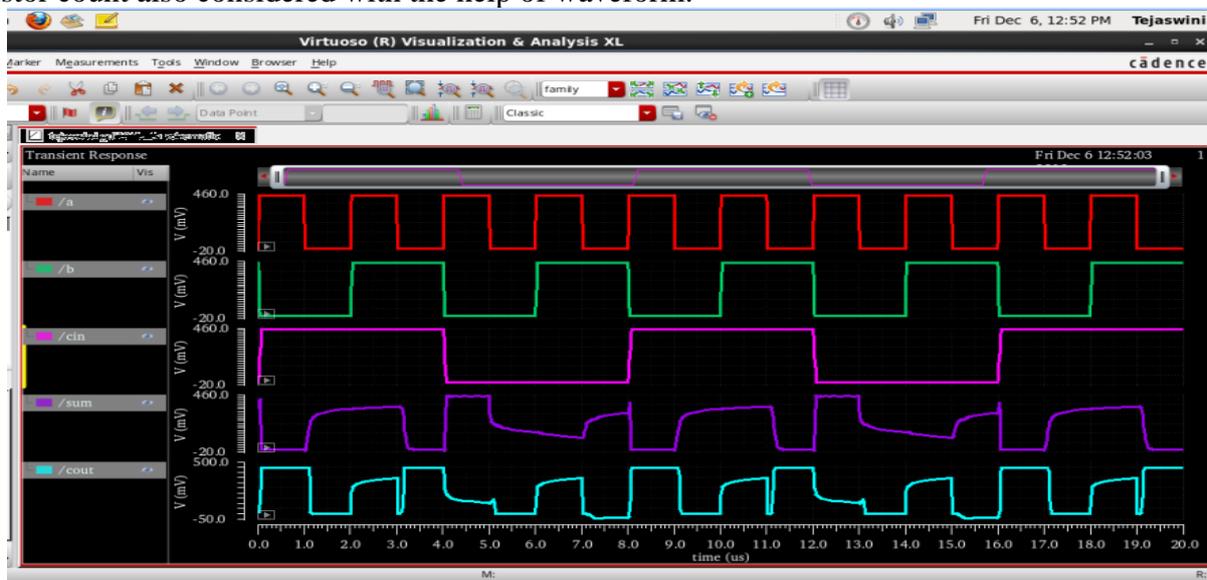


Figure. 5. Waveform of 8T MGDGI full adder

#### 5. Comparison:

Table. 1. Comparison of different full adder cells

Full adder	Average power	delay	Number of transistors
Conventional full adder	$448.3e^{-12}$	$2.03e^{-3}$	28
10T GDI	$142.5e^{-12}$	$42.50e^{-9}$	10
16T hybrid	$139.0e^{-12}$	$42.95e^{-9}$	16
14T MVT-GDI	$107.3e^{-12}$	$3.009e^{-6}$	14
8T MGDGI	$83.2e^{-12}$	$25.9e^{-9}$	8

## 6. Conclusion:

This paper mainly works on the MGDI technique and also execution of different full adders using GDI and hybrid techniques. The above table appeared as the comparison of dissimilar full adders. The simulation is done by using cadence tools. In the case of parameters like average power and transistor count the 8T modified gate diffusion full adder is better than the 14T MVT-GDI full adder, 10T gate diffusion full adder and 16T hybrid full adder. So the better 8T modified gate diffusion input full adder and it is best outfitted for low power applications. The extension and future scope of this paper is to uses these types of full adder in any multipliers and adders.

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