Fastest Multiplier Implementation Using Ancient Scriptures Algorithms: Review

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Abstract

In any of the fastest ALU, multiplier play an inevitable role. There is always a demand on high speed multiplier due to the raising limitation on delay. Increasing the speed of a multiplier there are number of new techniques have been implemented in which multiplier using Vedic mathematics are foremost one. Vedic mathematics are derived from ancient Vedas, it is mainly divided in to 16 sutras and upasutra in which Urdhva Thiryagbhayam and Nikhilam sutra are used for multiplication. Multiplier are used in different area such as cryptography, image processing application, embedded system application, programmable filter application etc. The multiplier efficiency are depended on their speed, delay and area. In this article different multiplier are compared with their efficiency and concluded that Vedic multiplier are most prominent among them.

Keywords: Urdhva Thiryagbhayam, Nikhilam sutra, Delay, Area, Multiplier

1 INTRODUCTION

Indian system of mathematics played a major role in ancient sculptures. Jagadguru Shri Bharathi Krishna Tirthaji was the person who rediscovered the Vedic system of mathematics in beginning of 20th century. Conventional mathematics contain more complex and tedious process for problem solving, it can reduce by using Vedic mathematics. Vedic mathematics are incorporated with 16 sutras and 13 upasutra. Vedic mathematics can apply to any area of mathematics example Integral, differential, geometry, trigonometry, addition, multiplication, division, root of the equation etc. Era of digitalization make high challenge on high speed digital circuit. High speed can achieved only through the high speed processor. Any of the processor speed can depend on the multiplier used on it. Multiplier is an essential part for any computation process. Conventional multiplier (Booth, Array, and Wallace Tree) can provide less efficiency in area, speed and power. For improving the efficiency of the multiplier, it can design using Vedic algorithm. Vedic algorithm can include less number of steps for multiplication so that efficiency of the system can increase. In this paper we make a survey on high speed Vedic multiplier.

2. Related Work

V.S Kumar Chunduri et al. [1] proposed an 8bit Vedic multiplier using Urdhva Thiryagbhayam algorithm in which analysis can be done using Xilinx hardware tool. This paper shows that the 8 bit Vedic multiplier has low power 82nW and high speed 145.03MHz as compared to conventional multiplier. The proposed multiplier shows high performance on higher order bit. G. Ganesh Kumar et al. [2] implemented a 32x32 bit multiplier using Vedic algorithm .32 bit multiplier can produce a delay of 31. 52ns compare to conventional multiplier it concluded that Urdhva Thiryagbhayam, Nikhilam and Anurupye sutras are reduce the delay, power, and hardware requirements of multiplier compare to conventional multiplier.
Nishant G et al. [3] offering a 32x32 bit Vedic multiplier. In this paper multiplier attain a smaller delay of 6.46ns by using UT algorithm. For future work an integrated Vedic ALU is proposed for this article. And it concluded that Vedic multiplier are more efficient in terms of speed compare to other multiplier.

Ramachandran S et al. [4] designed an integrated Vedic multiplier architecture, in which multiplier architecture itself select the proper multiplication sutra. This will done through the applied input .If input is larger number of bit design selected the faster algorithm of Nikhilam Sutra, if input is smaller number of bit it selected the Urdhva Tiryagbyham.

Surabhi Bhardwaj et al. [5] discovered an advance Vedic multiplier. In which basic multiplication can done using Urdhva Tiryagbyham algorithm and accumulation process can done using Carry Select Adder. Compared to other16 bit multiplier proposed multiplier shows less delay of 30.659ns.

Beechu Naresh [6] designed a new multiplier especially for squaring application. It outcomes concluded that, this architecture is worth for high performance processor.

Prasanth D Pawel et al. [7] gave implementation of new Vedic multiplier using UT algorithm and CLA adder addition method. In which it seen as high efficiency in speed and area compared to existing method.

Hemangi P Patil et al. [8] proposed a new multiplier using Vedic algorithm and reversible logic. It showed that Nikhilam sutra using reversible gates can provide a high efficiency in terms of power, area and delay compared to conventional Vedic multiplier and Booth multiplier.

S Arish et al. [9] find out that combination of Karatsuba algorithm and Urdhva Tiryagbyham algorithm of a multiplier shows percentage of reduction in area and delay when number of bit length is increased.


Praveen Kumar Y G et al [11] make a study on different multipliers papers and he concluded that multiplier using UT Vedic algorithm is more prominent among power and speed compare to conventional multipliers.

<table>
<thead>
<tr>
<th>No.</th>
<th>Title of the Paper</th>
<th>Publisher/year</th>
<th>Algorithm or Method</th>
<th>Inference</th>
<th>Tool used</th>
<th>Efficiency based on power, delay, speed</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Design and implementation of multiplier using KCM and Vedic mathematics by using reversible adder</td>
<td>IJME R 2013</td>
<td>Urdhva Tiryagbyham with reversible adder</td>
<td>Vedic Multiplier using reversible adder can provide a better performance in higher order multiplication</td>
<td>Modelsim and Xilinx spartan3E, FPGA kit</td>
<td>Area=180 Speed=145.03MHz Power=82 mW (8x8 bit)</td>
</tr>
<tr>
<td>2</td>
<td>Design of high speed Vedic multiplier using Vedic mathematics techniques</td>
<td>IJSR P 2012</td>
<td>Urdhva Tiryagbyham algorithm</td>
<td>Multiplier using UT algorithm provide minimum delay for multiplication in any type of input bit</td>
<td>Xilinx Spartan XC3S500-5- FG320</td>
<td>Delay=31.526ns (32x32 bit)</td>
</tr>
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<td>3</td>
<td>Ancient Indian Vedic Mathematics based 32-Bit Multiplier Design for High Speed and Low Power Processors</td>
<td>IJCA 2014</td>
<td>Urdhva Tiryagbyham algorithm</td>
<td>Complexity of the hardware can reduced for higher order input bit by using Vedic multiplier</td>
<td>Modelsim Xilinx Virtex5 (XC5V LX110T)</td>
<td>Delay=6.465ns (32x32 bit)</td>
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<td>No.</td>
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<td>4</td>
<td>Design implementation and performance analysis of an integrated vedic multiplier architecture</td>
<td>IJCR 2012</td>
<td>Urdhva Tiryagbhym and Nikhilam sutra</td>
<td>Xilinx ISE 11 Speed 32.816ns for 64bit 13.455ns for 8bit</td>
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<td>5</td>
<td>Design of High Speed Multiplier using Vedic Mathematics.</td>
<td>IJER 2014</td>
<td>UT algorithm for multiplication and Carry Save Adder for accumulation</td>
<td>Modelsim Xilinx Spartan 3 Xc3s50-4 Delay= 30.659ns (16x16 bit)</td>
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<td>6</td>
<td>Design and implementation of high performance and area efficient square architecture using Vedic Mathematics</td>
<td>Analog integrated circuit and signal processing 2019</td>
<td>Anurupye Sutra</td>
<td>Vivado design suite 2018.3k intex-7 FPGA Delay= 38.6ns (64x64 bit)</td>
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<td>7</td>
<td>High speed Vedic multiplier design and implementation on FPGA</td>
<td>IJAR 2015</td>
<td>UT algorithm with compressor and CLA adder</td>
<td>Xilinx XC3s200-4tq.144 Area are represented by number of LUT used 679</td>
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<td>8</td>
<td>FPGA implementation of conventional and vedic algorithm for energy efficient multiplier</td>
<td>IEEE 2015</td>
<td>Nikhilam sutra with reversible logic</td>
<td>Xilinx Spartan 3E 3s250e VQ-100 FPGA Delay= 8.73ns Power= 82mW</td>
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<tr>
<td>9</td>
<td>Run-Time-Reconfigurable Multi-Precision Floating-Point Matrix Multiplier Intellectual Property Core on FPGA</td>
<td>Circu it syste m and signa l proce</td>
<td>Karatsuba algorithm and Urdhva Tiryagbhym algorithm</td>
<td>Xilinx ISE 14.7 Virtex 5 ML10 Delay= 11.514ns (16x16 bit)</td>
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<td>10</td>
<td>A modular Vedic multiplier architecture for model-based design and deployment on FPGA platforms</td>
<td>Microprocessors and Microsystems 2020</td>
<td>Urdhva Tiryagbhyam algorithm With 4:2 compressor</td>
<td>This design shows a better performance in area and delay compare to Wallace tree, Booth and 4:2 compressor reference multipliers.</td>
<td>Xilinx VIVADO Artix 7 FPGA.</td>
<td>Number of LUT used in 32 bit multiplier =1086</td>
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Table 1: survey of high speed multiplier using Vedic mathematics techniques

3 CONCLUSION

In this survey we focused on the various type of Vedic multiplier and it shows a high efficiency in speed, delay and power compare to conventional multipliers. These multipliers have a large application in many areas such as Dsp, Fft, Filters, Biomedical application, image processing and also in cryptography.

REFERENCE


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