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THERMAL ANALYSIS OF THROUGH SILICON VIAS USING MWCNT BASED TSV IN 3D INTEGRATED PACKAGING SYSTEM

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Abstract. In this paper, a four die stacked 3D ICs with integrated multi walled carbon nanotube (MWCNT) based through silicon via (TSV) is constructed. The steady state thermal-electric analysis is performed. The current density and the equivalent stress analysis is performed along the TSV path. ANSYS workbench is used for the simulation. The average stress values and current density values are evaluated at various applied currents and are compared. The total deformation for the both MWCNT based TSV and Copper based TSV are compared. It shows that CNT based TSVs outperforms copper based TSVs.

1. Introduction

3D IC stacking technology is quickly developing technology in the field of semiconductor industry, which expands by stacking 2D IC multiple circuit layers in vertical way [1-4]. This 3D IC stacking technology helps in reducing the Power dissipation, delay, packaging size and total wire length [5-7] contrasted with 2D IC technology. On the other hand, due to the power density and rising operating frequency it causes severe heat problems. Therefore, in order to overcome heat problems the thermal management is necessary [8].

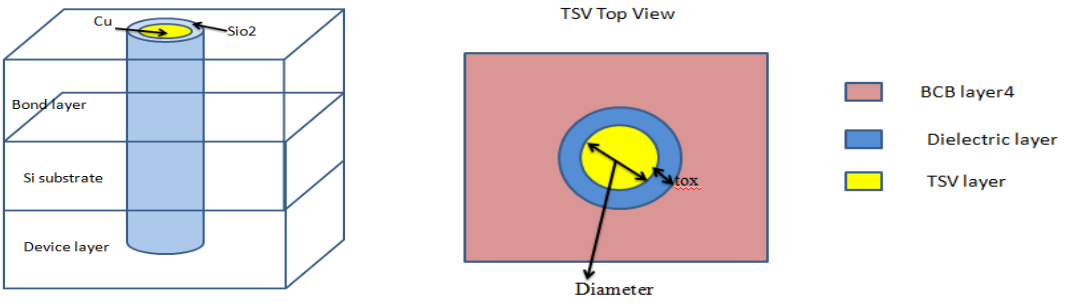
Among different 3D Integrated circuit techniques, a TSV based 3D IC has been very much thrived and actualized in numerous mechanical applications [9]. TSVs are integrated in 3D-IC, which connects the top and bottom layers of a chip to transfer information. TSV based 3D IC helps in maintaining and managing higher number of input and outputs, it helps in decreasing wire length and better throughput. Copper is being used as a primary filler material for TSV interconnects. At excessive temperature and high operating frequency, TSVs experiences electro migration and skin effect [10-11]. In addition, CTE mismatch between silicon and copper causes thermal stresses [12]. This pattern is pushing specialists to discover trade for the material.

Recently, carbon Nanotubes (CNTs) has attracted a lot of thought due to its physical properties such as current carrying capabilities, high thermal conductivity and mechanical stability [13-20]. In this paper, the thermal stress analysis is performed for a 3D –IC using copper and MWCNT as a filler materials. The Equivalent stress analysis was performed at various current and temperatures. The deformation of TSV at various current values is evaluated.

2. TSV Geometry

The physical structure of TSV is depicted in the Fig. 1. It contains a conducting material through the different layers of a four die stacked TSV model from one end to opposite end which surrounds by a dielectric material in Fig. 1(a). TSV is surrounded by the three layers such as device layer, Si substrate layer and bond layer, where the hole is etched through the four die stacked model. TSVs can be filled with conductive material. TSV needs dielectric layer for satisfactory separation to the encompassing Si substrate.

Figure 1(b) shows the top view of TSVs. The dielectric material is considered as SiO_2. For isolation, the TSV layer is encased with the dielectric layer. But, at high temperature the due to the large coefficient of thermal mismatch usually occurs between Si and copper in TSV during thermal cycling leads to the thermo mechanical stress. The electro migration effects will be caused due to the thermo mechanical stress. The thermal stress further leads to the damage of the device. Due to the restriction in the current carrying capability and thermal conductivity it experiences difficulty to grow in vertical direction. CNT can overcome these problems because of its unique physical properties and mechanical strength it is better filler material than copper. The CNT can handle high the high thermal conductivity and current density respectively.



(a) (b)

Fig. 1. (a) Four die stacked TSV model (b) Top view of TSVs.

3. Simulation Results

In this section, the model of four die stacked chips with copper and MWCNT based TSV are investigated. The power supply is applied at the top of the TSV. Using finite element analysis, the entire TSV is modeled with 3D thermal structure is shown Fig. 2.

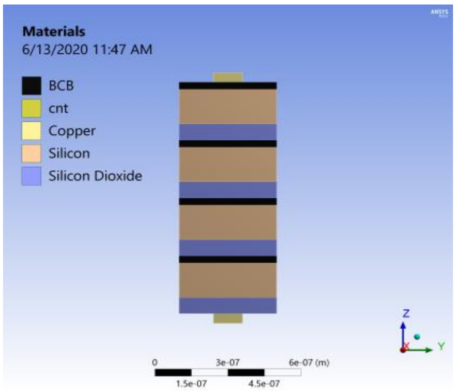


Fig. 2. Four die stacked TSV structure

Moreover, ANSYS workbench simulations [21] was used to verify the experimental results. As per ITRS [22], the dimensions of the device layer, Si layer and bond layer are

0.07µm, 0.15 µm and 0.03µm respectively. TSV diameter, TSV length and Sio2 thickness are 0.1µm, 0.1µm and 0.01µm respectively. In addition, the filler material properties are mentioned in Table 1.

Table 1. Materials and their properties

Material	Density ($kg\ m^3$)	Young's modulus (Pa)	Poisson ratio (Pa)	Conductivity ($wm^{-1}k^{-1}$)	Resistivity (Ω.m)
BCB	957	6.1×10^{9}	0.35	0.29	1×10^{19}
Copper	8933	1.115×10^{11}	0.343	400	1.673×10^{-8}
Silicon	2330	1.62×10^{11}	0.28	148	640
SiO_2	2220	7.17×10^{10}	0.16	1.5	1×10^{19}
MWCNT	1400	1×10^{12}	0.3	3000	1.74×10^{-8}

3.1. Current density of TSV

In the TSV the high current density leads to electro migration which is the major issue. The electro migration degrades the performance of the chip. In order to examine the TSV performance, the current density and corresponding stress values are evaluated for copper and MWCNT based TSVs. Table 2 shows that the current density and corresponding stress values of copper and MWCNT based TSVs. As the current increases the current density and stress values also increases in both the cases. It is noticed that the stress values of copper based TSV are higher than MWCNT based TSV due to mismatch of CTE. For an instance, at applied of 2A, the stress values of MWCNT based TSV is 16.68% lesser than copper based TSV.

Table 2. Average Current density and equivalent stress value of copper and CNT based TSV

Current (A)	**Cu based TSV**		**CNT based TSV**	
	Current density (A/m^2)	**Stress (Pa)**	**Current density (A/m^2)**	**Stress (Pa)**
1	1.2634×10^{14}	2.5116×10^{10}	1.2637×10^{14}	2.0941×10^{10}
1.5	1.8951×10^{14}	5.6503×10^{10}	1.8955×10^{14}	4.7085×10^{10}
2	2.5269×10^{14}	1.0045×10^{11}	2.5274×10^{14}	8.3686×10^{10}
2.5	3.1586×10^{14}	1.5694×10^{11}	3.1592×10^{14}	1.3075×10^{11}

3.2. TSV deformation

Another way to examine the TSV performance is structure deformation. The structure deformation of copper and MWCNT based TSV is examined in this section. Figure 3 show that the structure deformations in copper based TSV as current density increases. It is observed that the current density increases, the four die stack structure of copper based TSV is deformed.

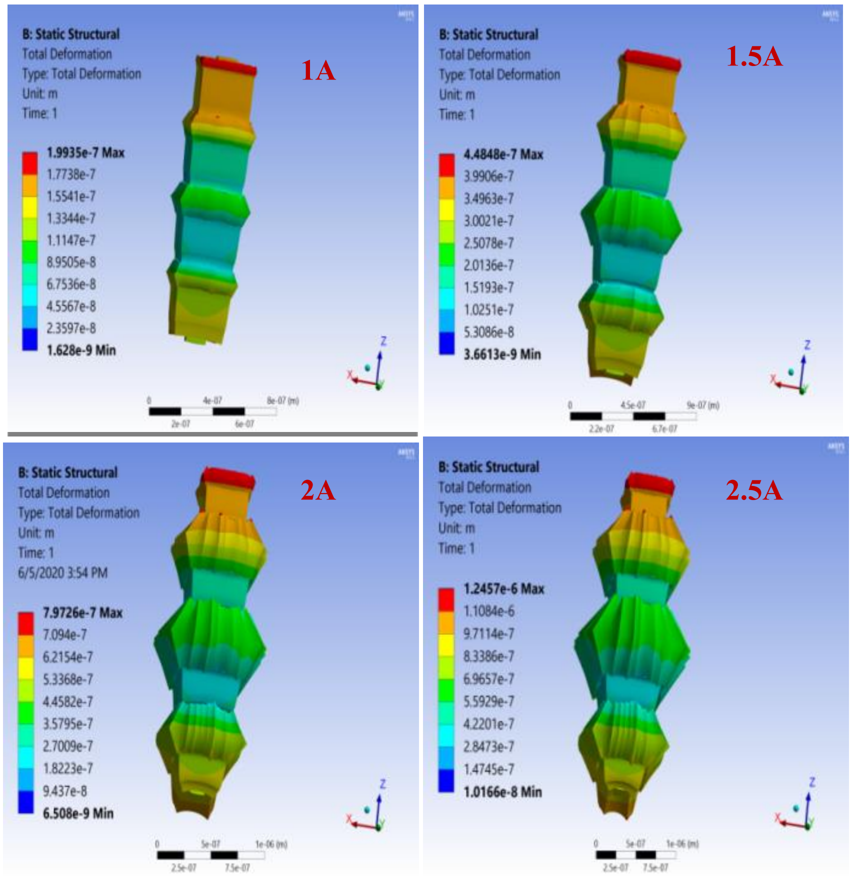
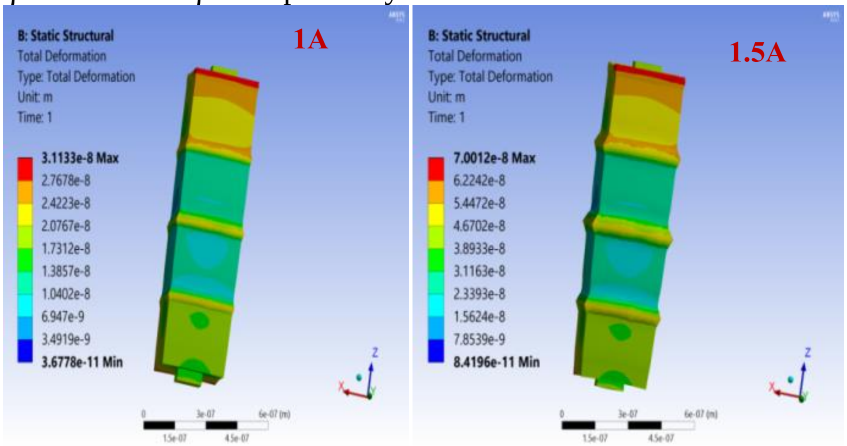


Fig. 3. Cu based TSV deformation with layers at current 1A, 1.5A, 2A, 2.5A respectively

It is due to structure deformation is directly proportional to stress. For example, at current 2.5A, the structure deformed 1.23553µm. Figure 4 illustrates the structure deformations in MWCNT based TSV. It is evident that less deformation can be seen in MWCNT based TSV than copper based TSV. On an average structure deformations in copper and MWCNT based TSVs are 0.667 µm and 0.375 µm respectively.



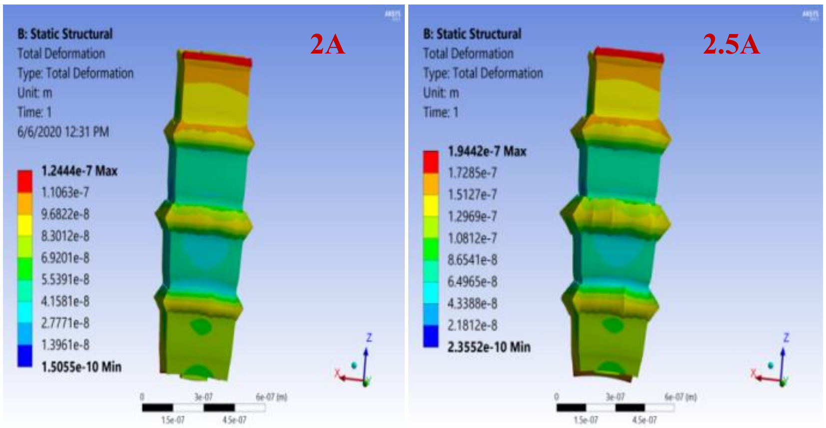


Fig. 4. MWCNT based TSV deformation with layers at current 1A, 1.5A, 2A, 2.5A respectively

Therefore, it can be concluded that MWCNT based TSV outperforms copper based TSVs. CNT is best suitable filler material for futuristic TSV based 3D ICs.

4. Conclusion

This paper presents the thermal and electrical analysis for 3D-IC integrated with Cu based TSV and MWCNT based TSV. Here, the current density, equivalent stress analysis for copper and MWCNT based TSVs are performed. The simulation results proves that the CNT can be replaced as a filler material of TSV interconnect because, it can transfer heat effectively than copper. MWCNT has good yield and better elasticity compared to copper. In addition, the structure deformations are less noticeable in case of CNT based TSVs.

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