Design of 24 Bit Vedic Multiplier Using GDI Technique in 32 Bit Floating Point Multiplier

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Abstract: Multiplier is the common hardware block present in any processor. Floating point multiplier's can be found in electronic systems that run complex calculations especially in DSP processor. The Floating point numbers are commonly used in numerous applications because of their effective capability in representation of numbers. The feasible way of presenting real numbers in binary format is done by using FP numbers. A 24 bit Vedic multiplier using GDI technique is designed in this paper. Multiplication of two numbers will take more time and many steps. For the unsigned mantissa multiplication in the FP multiplier the Vedic mathematics sutra called UT is used. Any logic circuit can be designed by using CMOS logic. The CMOS logic will consumes more area. The numbers of transistors in the circuit are reduced by using GDI logic. Thus the Vedic mathematics will reduce the delay and the GDI logic will reduce the transistors count in a circuit which in turn reduces the power.

Keywords: Floating Point, GDI Technique, Vedic Mathematics.

1. INTRODUCTION

In the present applications Fixed-point calculations is easy to operate but the floating point calculations has its own importance with better precision and higher dynamic range. Floating point arithmetic has its important applications in digital signal processor and also all computer systems are supported to it. There is a standardized format for representing the floating point numbers, it is called IEEE-574 format. Single precision (binary32) format and double precision (binary64) format are used in representing the floating point numbers. Single precision format is divided into 3 units, which are mantissa, exponent, sign. The structure of single precision format is shown in fig.1.In single precision format the mantissa part has 23 bits and one implicit exclusive bit '1' in MSB for normalization from 0 to 22,from 23 to 30 the 8 bit exponent unit is represented, last bit is sign bit which is 31st bit.

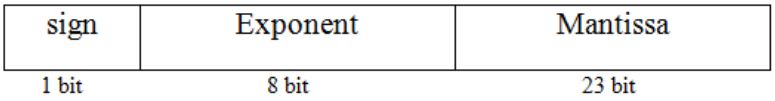


Fig. 1 Single Precision Floating Point Format

In a FP multiplier [1] multiplication of two numbers in IEEE754 format is performed in three steps. First step is 24 bit mantissa multiplication, and the second step is 8 bit exponent addition and the obtained exponent is converted into excess 127 format and sign bits are XOR ed to get the resultant sign bit. In the third step the output from the multiplier and the

adder are given to the normalizer to get the required output. In this paper the Vedic multiplication and GDI techniques are used for the 24 bit mantissa multiplication.

To design a mantissa multiplier in circuit level, a proper logic design such as the CMOS logic, transmission gate, or GDI technique can be used to minimize parameters like area, power which are important for a circuit performance. In CMOS devices the noise immunity is very high and the static power consumption is low but more area is required. Hence, there is a requirement for logic to save area.

Work on combination of Vedic multiplication and GDI logic is used to design a 24 bit multiplier in a single precision floating point multiplier[2] has presented. In section 2 introduction to floating point multiplication. Vedic mathematics in Section 3. In section 4 introduction to GDI logic is presented. Results are present in section 5.Conclusion is given in section 6.

2. ALGORITHM FOR MULTIPLICATION IN FP MULTIPLIER

The multiplication in FP numbers can be done mainly in four different steps.

1. Sign bit calculation.
2. Exponent calculation.
3. Mantissa multiplication.
4. Control block to check normalization.

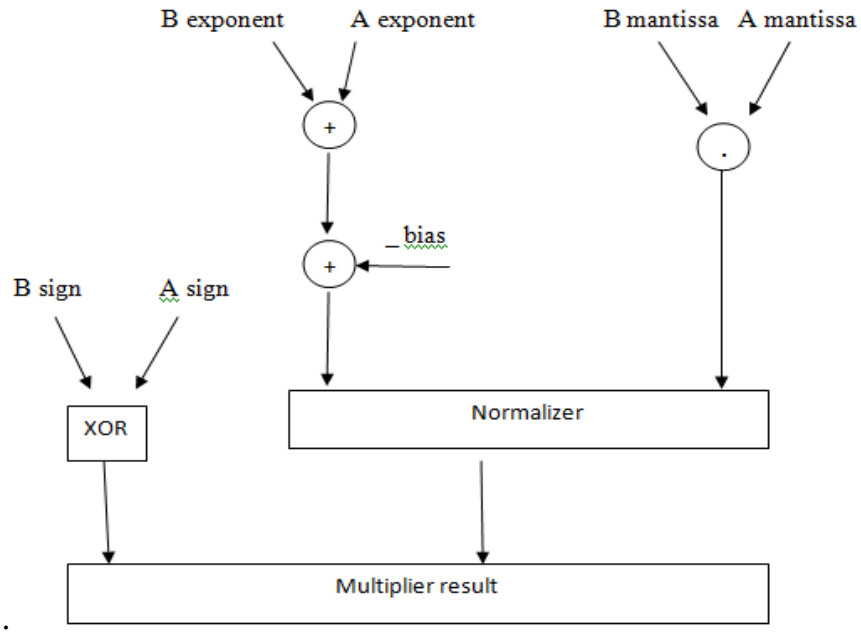


Fig. 3 Floating point multiplier block diagram

A 24 bit multiplier is present in mantissa multiplier unit which will multiply 2 numbers and the result is given to the normalizer unit. In this paper an efficient use of Vedic Multiplication and GDI techniques are used for the design of 24 bit multiplier has presented.

3. VEDIC MATHEMATICS

In ancient times the Indian Mathematics is names as Vedic Mathematics. The Vedic mathematics was again finding from the Vedas by Sri Bharati Krsna Tirthaji (1884-1960) between 1911 and 1918. According to all his research, there are sixteen Sutras in Vedic mathematics

[3]. According to him the Coherence is the prominent characteristic of the Vedic mathematics and it is easily understandable. Thus, mathematics is made easy, enjoyable and it motivates for new ideas. Therefore, by using Vedic methods the huge sums or 'difficult' problems are easily solved. Vedic Mathematics is applied in fast calculations like multiplication, division, squaring, cubing and some other. A highly efficient approach is provided by Vedic Mathematics to cover a more range from elementary multiplication to relatively advanced topics.

3.1. “Urdhva-tiryakbyham” Sutra

For any multiplication types “Urdhva-tiryakbyham” Sutra is applicable to all. Using line diagram multiplication of two 2 digit numbers and two 4 digit numbers is shown in Fig.4 (a) and fig.4 (b) respectively. In Urdhva Tiryakbyham method the numbers from two sides of the lines are taken and multiplied and obtained carry from before step is added. In the first step the resultant bit and a carry is produced. In second step the obtained carry will be added and the process repeats. After that all the obtained results are summed to the preceding carry, when more than one line is there in one step. Result bit is the least significant bit obtained in each step and remaining bits are given as carry for the second step. In the beginning we need to take carry as zero.

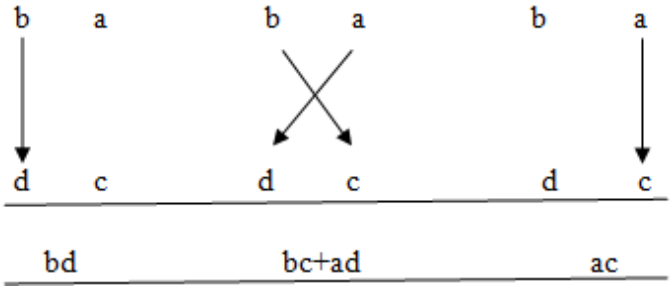


Fig. 4(a) 2*2 Vedic multiplication

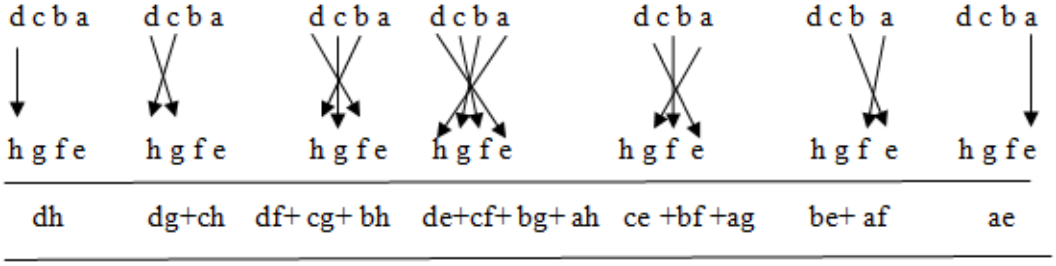


Fig. 4(b) 4*4 Vedic multiplication

4. PROPOSED MULTIPLIER DESIGN

The proposed 24 bit mantissa multiplier in IEEE 754 single precision FP multiplier is implemented using Vedic mathematics based on Urdhva Tiryakbhyam sutra and GDI technique. The proposed mantissa multiplier a 4*4 Vedic multiplier using GDI technique is used as a base block which is shown in figure 5. By using this base block a 24 bit Vedic multiplier[4] using GDI technique is designed for mantissa part multiplication.

a. 4 bit Vedic multiplier

Architecture of 4 bit VM[5] module is shown in fig5. Half adder and full adder blocks are present in the multiplier. In this paper these adders are designed using GDI logic. In 4X4 multiplication, consider the inputs as A and B which are of 4 bits each. Multiplier output will be of 8 bits as – S0 to S7.

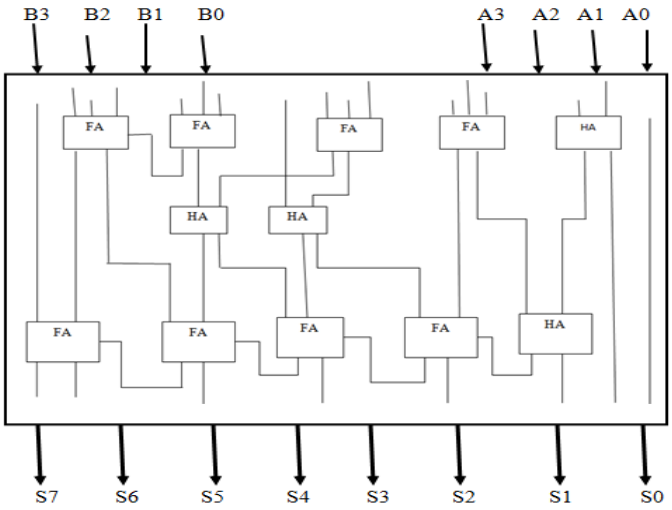


Fig. 5 Architecture of 4 bit Vedic multiplier

The 4*4 Vedic multiplier schematic is shown in the below figure. Input from a0 to a4 and b0 to b4 are given. These are given by using AND gate which is designed by using GDI technique. The outputs from the gates are given to the respective full adders and half adders. The corresponding outputs from s0 to s7 are taken.

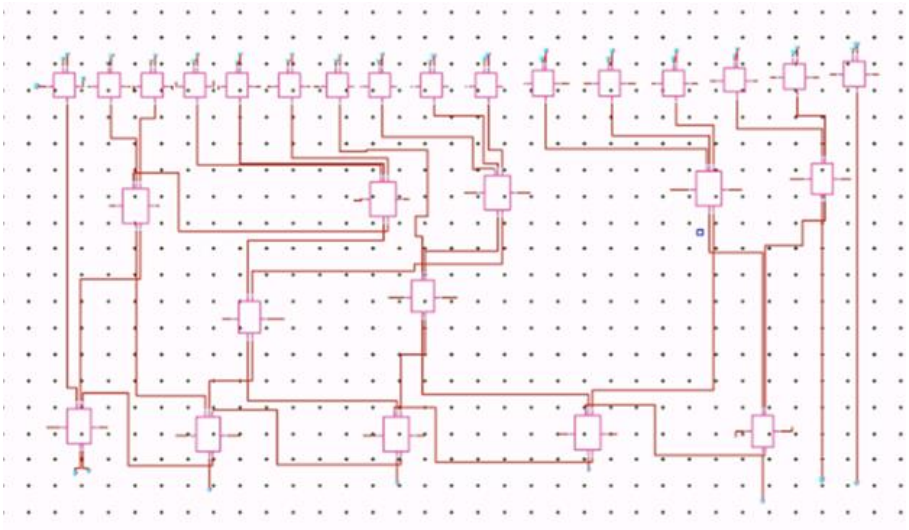


Fig. 6 4*4 Vedic multiplier schematic

b. 8 bit vedic multiplier design

The architecture of 8*8 VM is shown in Fig. 6.The 8 bit multiplier[6] design contains four 4*4 Vedic multiplier modules. Let's consider 8x8 multiplications, say the inputs A ranges from a0 to a7 and B ranges b0 to b7. The multiplier output will be of 16 bits as – s0 to

s15.Consider an 8 bit multiplicand, in that A can be split into pair of 4 bits that is higher and lower bits (AH-AL). In the same way multiplicand B can be split into BH-BL. The outputs from 4x4 multipliers are given to the ripple carry adders and the addition is performed accordingly to get the final product. In this design three 8 bit Ripple-Carry Adders are needed as shown in Fig.6.The adders are the combination of full adders which are designed used GDI logic. The required outputs from the adders are taken as the 8 bit multiplier product outputs.

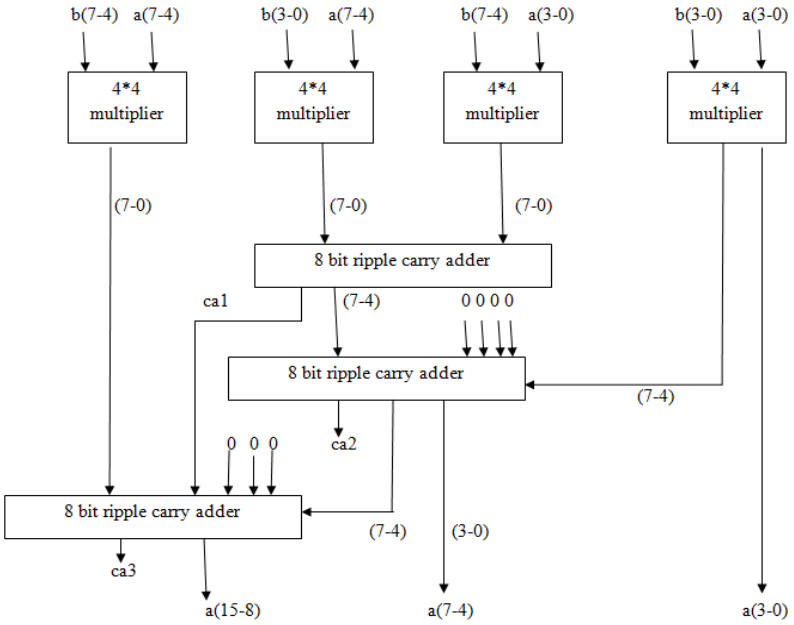


Fig. 7 design of 8 bit Vedic multiplier

Schematic output of 8*8 multiplier design is given in the figure below. The multiplier design will have four 4-bit Vedic multipliers and three adders each of 8 bit. The inputs from a(0-7) and b(0-7) are given and corresponding outputs from s0 to s15 are taken.

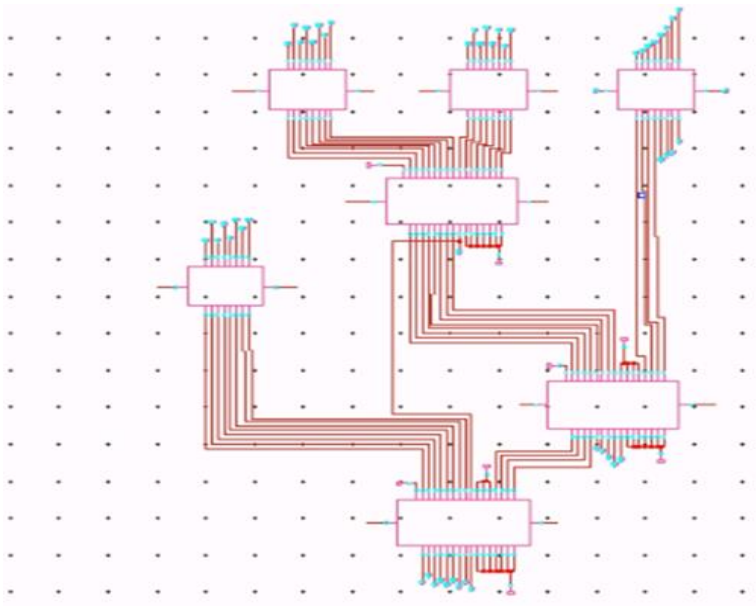


Fig. 8 Schematic of 8*8 multiplier

c. 24 Bit vedic multiplier design

The 24 x24 bit VM design[7] we need nine Vedic multipliers of 8 bit and five 16 bit and three 8 bit adders. Inputs are given from a0 to a23 and b0 to b23.the corresponding outputs are taken as s0 to s47.

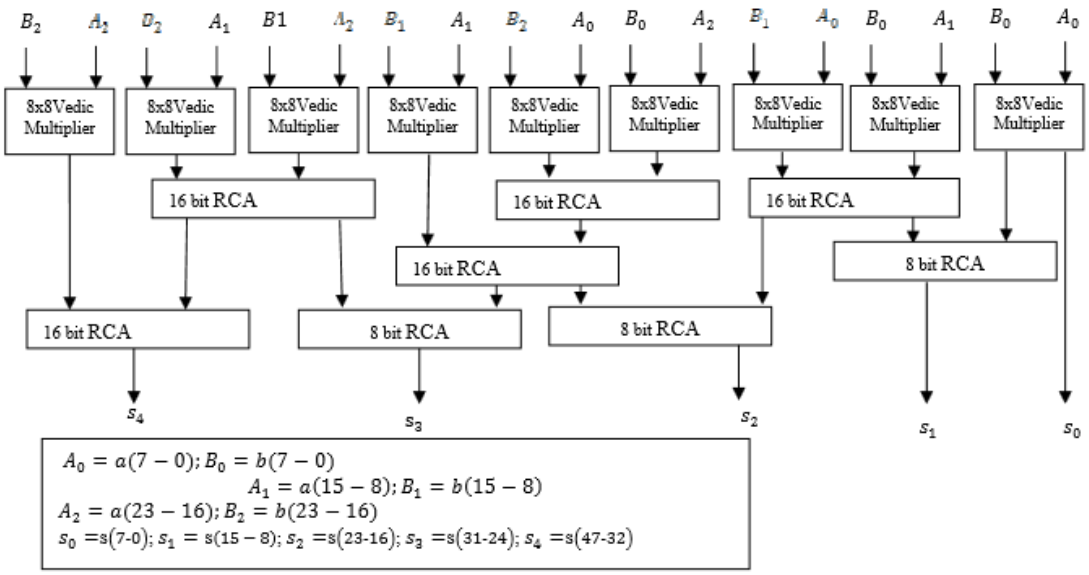


Fig: 9 24 bit multiplier architecture

The schematic of 24 *24 bit VM is shown in below figure. To design a 24 bit VM, nine 8 x 8 bit VMs and five 16 bit and three 8 bit adders are required. The inputs are given from a0 to a23 and b0 to b23.The corresponding outputs are taken as s0 to s47. 8*8 multiplier consists of 4 bit Vedic multipliers and the 16 bit adders and 8 bit adders are the full adders that are connected in parallel.

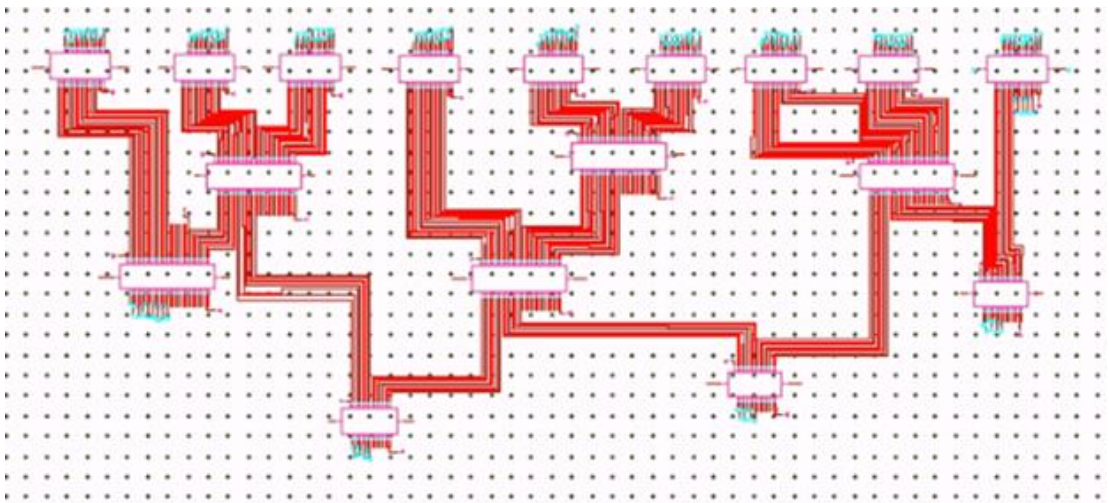


Fig: 10 Schematic output of 24*24 multiplier

4. GDI logic

In 2002 Morgenshtein [8] et al. invented the GDI logic. Figure 12 shows that the fundamental GDI cell comprises of two transistors. G, P and N are the three inputs of GDI cell. The output is taken from the drain terminals of both the transistors, and one of the input is taken from source terminal of p- type (pMOS) and the other input from is taken from source of a metal oxide semiconductor of n-type (nMOS). The nMOS bulk is connected to ground and the pMOS bulk is connected to supply voltage. Different functions implemented by using GDI logic are shown in table 1. GDI logic has a drawback that is the signal swing is reduced at the output. These signal levels can be restored by using buffers. Table 2 compares the logic circuits transistors count which is implemented by applying GDI (without buffer) logic and CMOS technique. Hence, by using GDI[9] logic any circuit will require fewer number of transistors when compared with other logics.

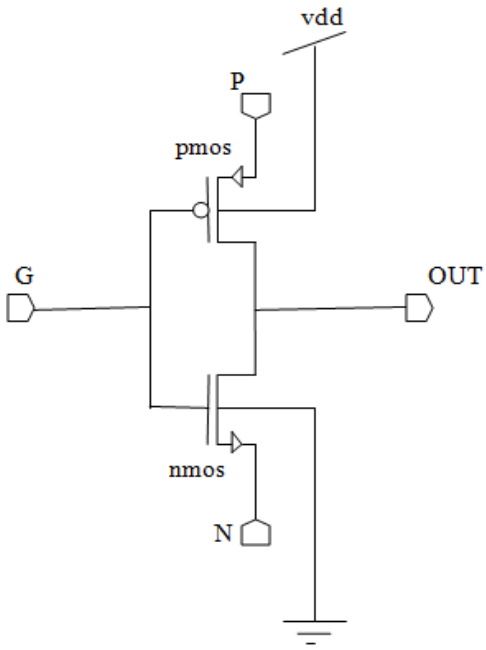


Fig. 11 GDI cell

Table 1: Different functions implemented using GDI technique

N	P	G	OUTPUT	LOGIC CIRCUIT
0	1	A	A'	NOT
B	0	A	AB	AND
1	B	A	A+B	OR
C	B	A	A'B+AC	MULTIPLEXER

Table 2: logic circuits TC in CMOS and GDI

Logic Circuit	GDI	CMOS
AND	2	6
XOR	4	12
Half adder	6	18
Full adder	10	28

The schematic output of XOR gate using GDI technique is shown in below figure. This GDI based XOR gate consists of only 4 transistors. Whereas the XOR gate designed by using CMOS logic will contains 12 transistors. The TC (transistor count) is less in GDI logic when compared to CMOS logic.

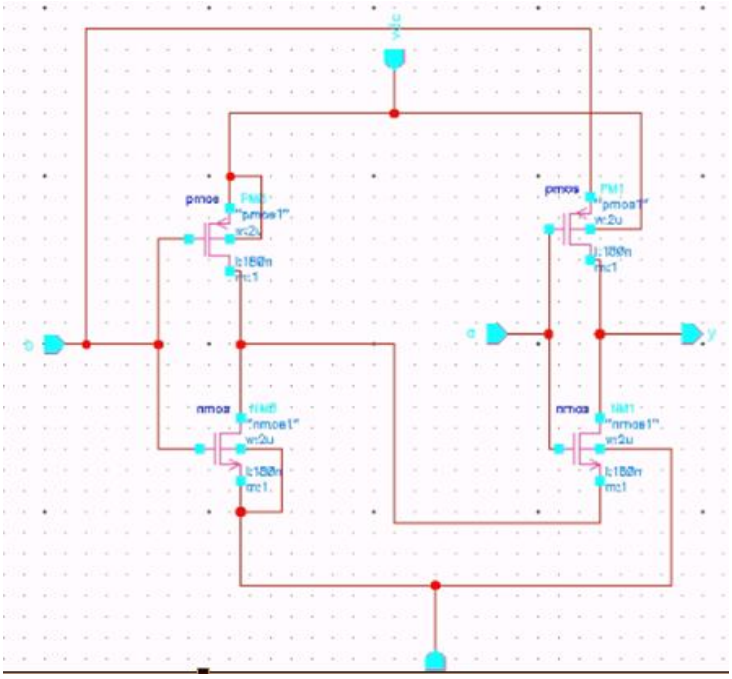


Fig. 12 Schematic output of GDI- XOR gate

Both the Vedic multiplication and GDI concepts are independently effectual. The delay in the circuit can be reduced by using Vedic multiplication technique and the transistor counts reduced by using GDI logic. As the TC is less dynamic power will be reduced. Hence, gate diffusion input based Vedic multiplier can be effectual.

4.1 GDI based full adder design:

In any ALU full adder is a fundamental block which is a nucleus to perform various operations like multiplication, subtraction, division, and address computation as well as additions. Full adders are encountered in the critical path of the complex arithmetic computation like multiplication. GDI based full adder [10] which operates on low power. The circuit level design of GDI based full adder with buffers is shown in figure 9.

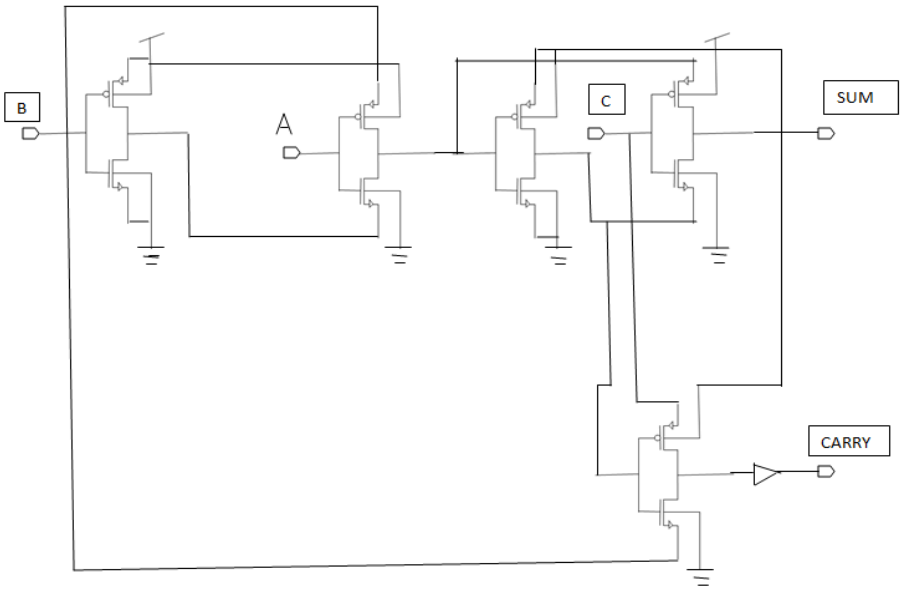


Fig. 13 GDI full adder

The schematic output of GDI based full adder is shown in the figure 14 which consists of p-type and n-type MOS transistors. A B and C are given as inputs and outputs are taken as sum and carry.

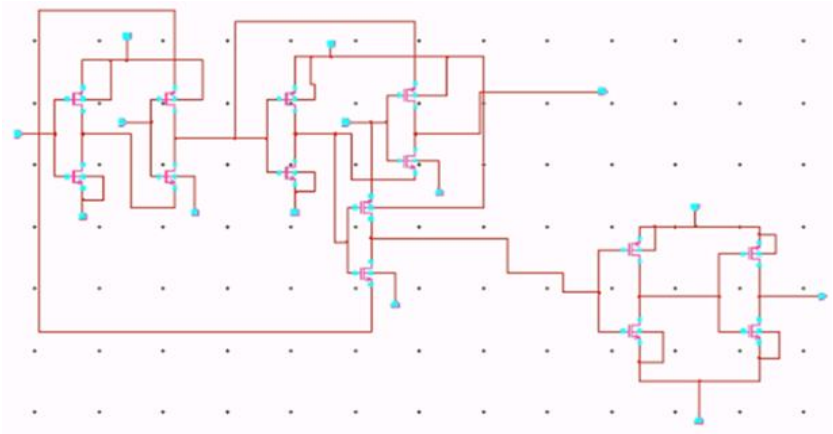


Fig. 14 Schematic output of GDI based full adder

5. RESULTS

The output wave form for GDI based XOR gate is shown in figure below. There are only 4 transistors required for a circuit to perform XOR operation using GDI logic. Also the output waveforms for the full adder and the proposed multiplier design are shown in below figures. The parameters like power, delay and transistor count are compared for the proposed multiplier and the conventional multiplier is shown in the table below.

Table 3: Comparisons of different designs using CMOS and GDI

Circuit	Power(nW)		Delay (ns)		TC	
	CMOS technique	GDI technique	CMOS technique	GDI technique	CMOS technique	GDI technique
AND	3582	2612	1.56	0.73	6	2

XOR	9530	3512	1.05	0.610	12	4
FULL ADDER	34427	1650	44.2	22.5	28	12
24 BIT VEDIC MULTIPLIER	10299	5428	12.6	5.3	19,616	8,160

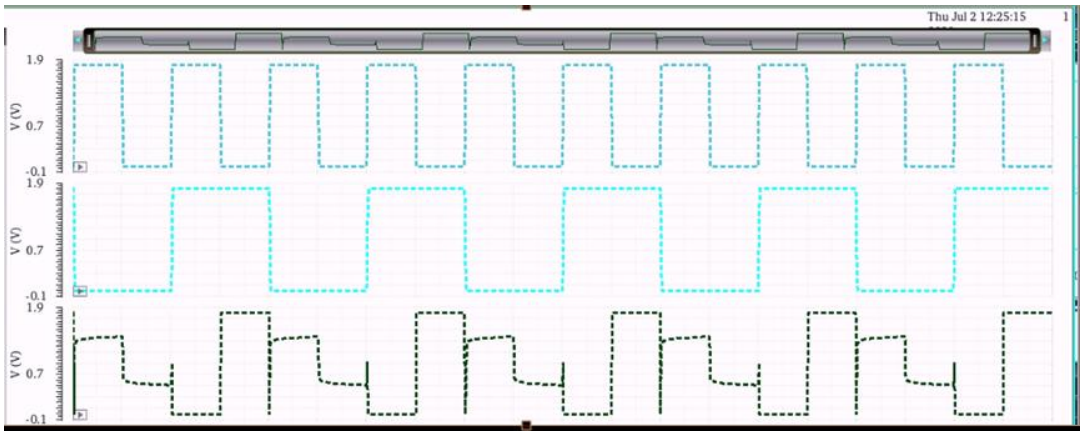


Fig. 15 GDI - XOR gate output

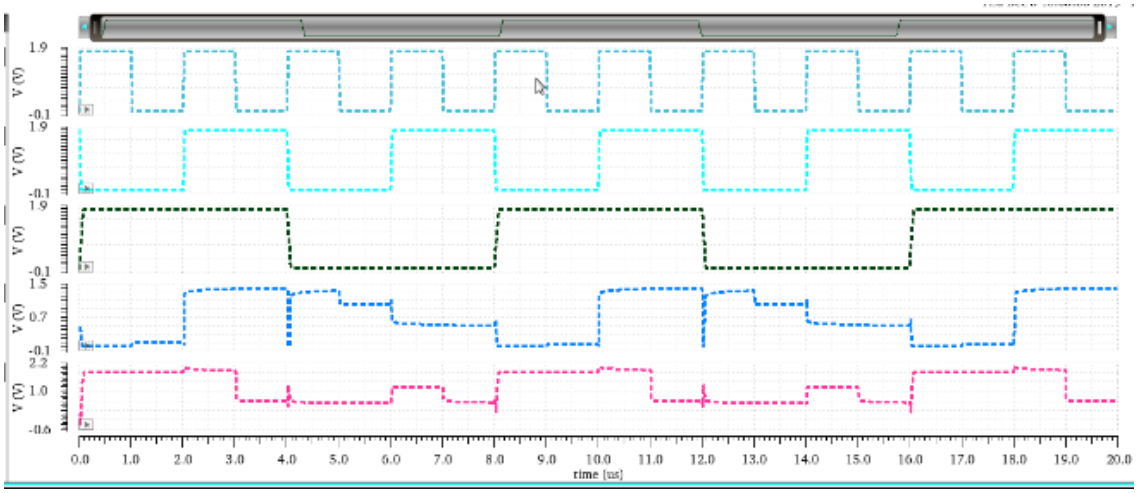


Fig. 16 GDI full adder output

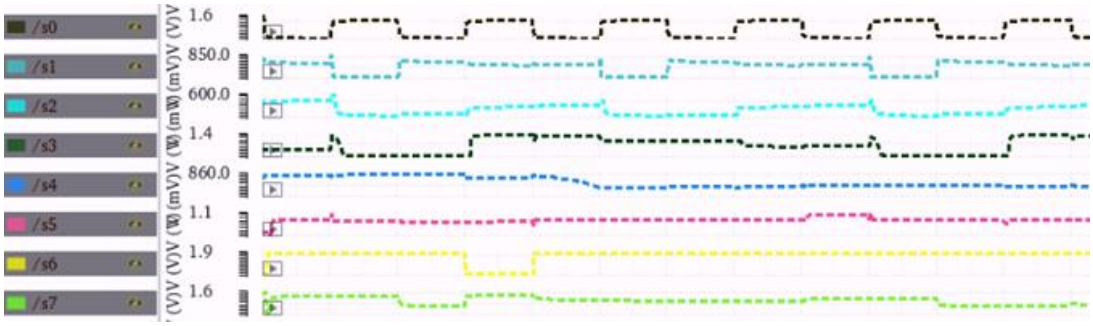


Fig. 17 Output waveform of 4 bit multiplier

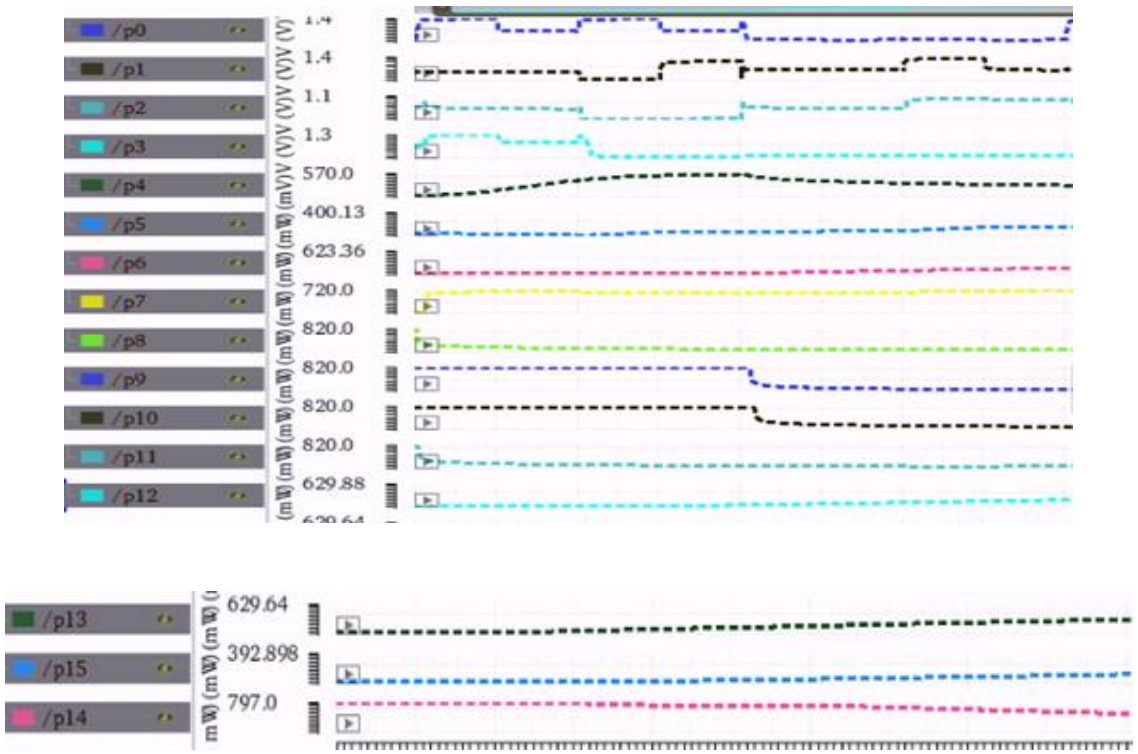
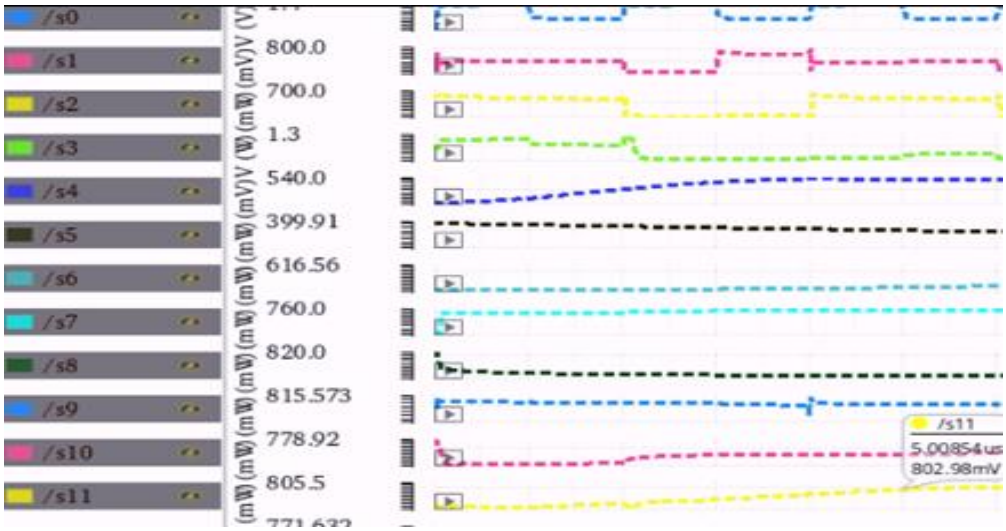
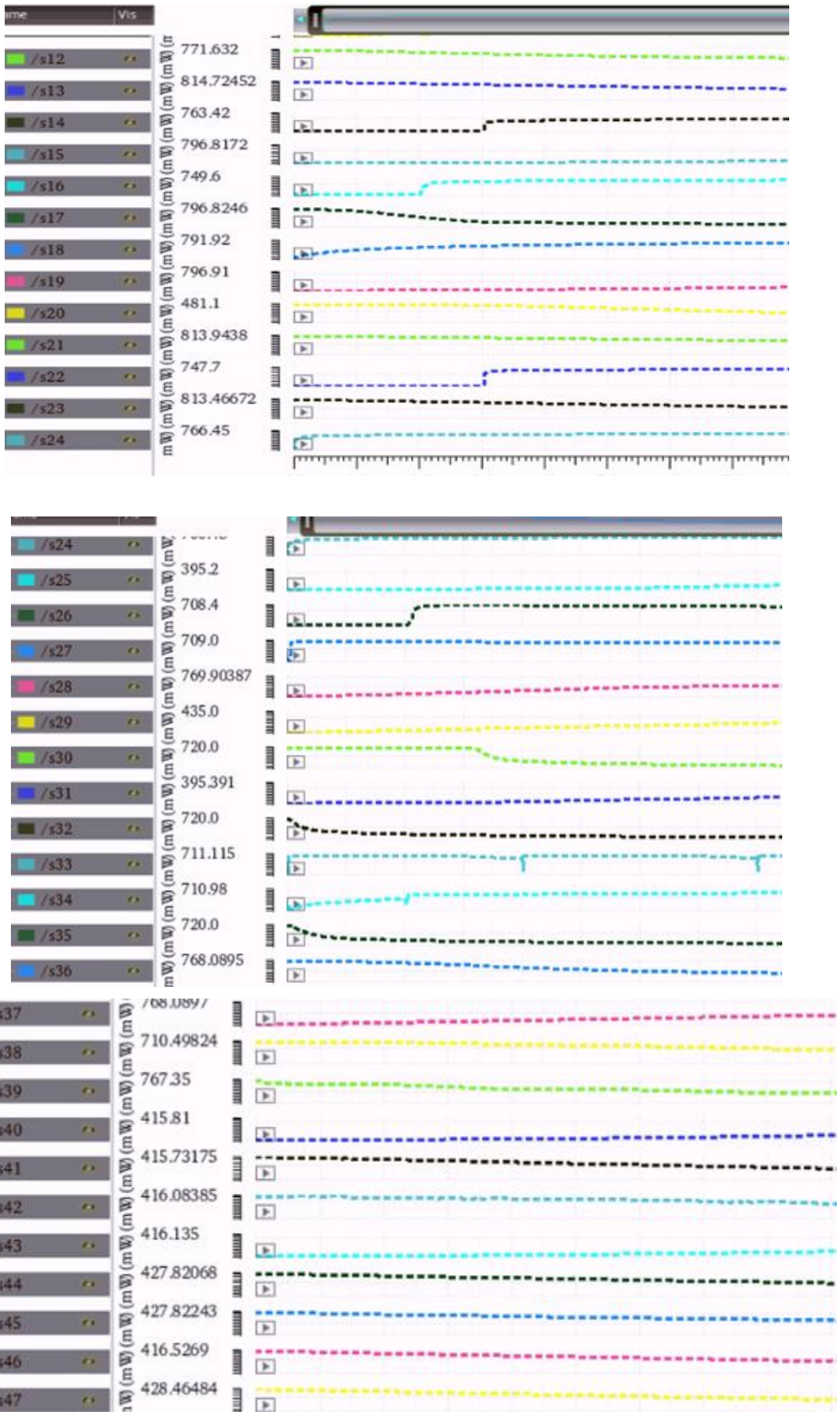


Fig. 18 8 bit multiplier output

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709.0
769.90387
435.0
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768.0895
/s37
/s38
/s39
/s40
/s41
/s42
/s43
/s44
/s45
/s46
/s47
710.49824
767.35
415.81
415.73175
416.08385
416.135
427.82068
427.82243
416.5269
428.46484

Fig: 19 Output of proposed 24 bit multiplier

6. CONCLUSION

In this paper the concept of Vedic multiplication and GDI logic are used to design a 24 bit Vedic multiplier in a 32 bit FP multiplier. The advantages of Vedic multiplication over the conventional multiplication and GDI logic over the CMOS logic are discussed. In the results parameters like power, delay, TC is less in proposed multiplier when compared to the conventional multiplier design. The proposed multiplier simulation and synthesis are done using cadence tool. In future the GDI based multiplier design will be help in designing of FFT systems and also floating point multipliers design.

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