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DESIGN OF 4-BIT MULTIPLIER ACCUMULATOR UNIT BY USING REVERSIBLE LOGIC GATES IN PERES LOGIC

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ABSTRACT —In VLSI circuits Heat is a major problem. However, in reversible logic, the measurement of heat dissipation is zero. In this sense, it is an important work in nanotechnology, low energy complementary metal oxide semiconductor structures [CMOS]. For reversible logic, no results are lost. However, this limits the delay in the scope of the hardware equipment. Therefore, reversible logic technology can be used to reduce energy distribution, reduce heat wave propagation and increase speed. Therefore, it is used to increase speed and reduce energy consumption. In this paper we are going to represent the following reversible logic gates, such as Fredkin gates, Peres, Feynman, Toffoli. This paper proposes a reversible logic design of a 4-bit MAC structure using Peres gates as reversible logic blocks. In addition, a variety of parameters, along with those of conventional computing, perform a relative test between classical style and quantum logic operation. The proposed approach is implemented using Xilinx-7 FPGA in VHDL.

Keywords: Reversible logic gates, Fredkin, Peres, Feynman, Toffoli, MAC, Array Multiplier and Ripple Carry Adder**.**

I.INTRODUCTION

Low power design has become a promising research area in IC design. Techniques for designing low-power circuits rely on choosing the best resources to slow down information processing without disturbing system characteristics. Designers of CMOS digital devices have challenging requirements. They need to optimize complex functions in combination with low propagation delay and low power consumption.

Today, in the field of integration, CMOS inverters play an important role in better designing VLSI technology NMOS and PMOS devices. In current technology, he may be preferred over many others, but low power and delay are becoming major obstacles for any designer to achieve a better way.

It is able to demonstrate high power consumption and high speed, and is growing to higher shapes and designs. It became a key issue in the final design as it achieves better results in terms of these parameters.

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designs. It became a key issue in the final design as it achieves better results in terms of these parameters.

Regarding this issue Researchers have been working from years to develop better designs and proposed a new designs to achieve high speed and low power consumption based on Reversible Logic.

Section II briefly describes about different reversible logic gates and their principles. Next III Section demonstrates on MCA Unit. Section IV demonstrate 4-Bit MCA Unit using reversible logic. Section V shows Simulation results of 4-Bit MCA Unit using Feynman reversible logic. Section VI describes conclusion and future work.

II.VARIOUS REVERSIBLE LOGICS

Reversible computing is Number of I / O lines provided individually mapping between input and output rows. In purpose of reversible computing eliminates that energy dissipation. It is generated by the destruction of information.

Reversible is a one-to-one circuit (gate) Mapping between input and output vectors. Thus, the input state vector is always Exit states vector. Reversible logic supports the process. How to run the system in both forward and reverse directions. This means Invertible calculation can generate input from output you can and go back to any point in the calculation history. Logic Gate with number of entrances equal to number an output to input and output mapping. In synthesis of reversible gate circuit, Deployment is not allowed as the one-to-many concept is not allowed reversible. However, the deployment of the reversible circuit achieved using an additional door. Reversible circuit must be designed with a minimum reversible Logic gate.

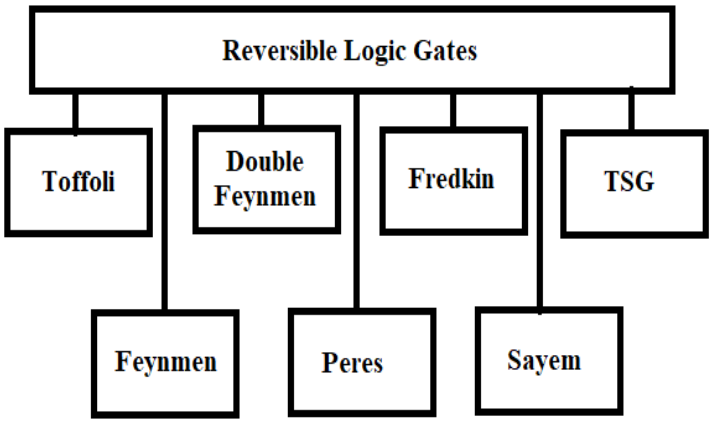

Fig. 1. Reversible Logic gates

The above Figure represent the different types Logics are available in Reversible gates.

III. MAC UNIT

A high speed and high throughput MAC unit is used to establish efficient digital signal processing system. The combination of multiplier, an accumulator and adder forms MAC unit which

gives low power dissipation. For getting high speed and low power consumption MAC unit can be designed using 4-Bit Reversible multiplier and 8-Bit Reversible Accumulator.

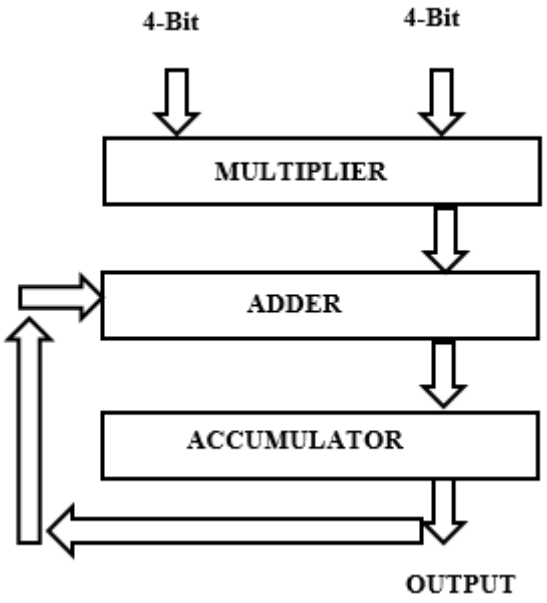

Fig. 9. MAC Architecture

By using the conventional multiplier, adder and an accumulator general MAC architecture can be formed. Where the output response is added to the previous MAC output result by an accumulate adder. Mainly in microprocessors and digital signal processors for data-intensive applications, such as convolution, filtering and inner products the Multiply-Accumulate (MAC) unit is used.

IV. IMPLEMENTATION

For the objective of get rid of undesirable equipment during handling the 4-Bit Reversible multiplier unit and 8-Bit Reversible snake and 8-Bit Reversible gatherer are utilized in the proposed MAC design.This improves the speed of operation of the MAC and also reduces the area.

Main purpose of using reversible multiplier instead of conventional multiplier is, this we notice a reduction in computations, basing on reduction of total number of operations. This factor gives proposed MAC unit design extra efficient compared to the existing one.in the proposed architecture by using limited hardware is established for only low power dissipation and fast operation.

A. 4 Bit Array Multiplier:

Below figure shows the 4 x 4 Bit array multiplier. Basic working principal is depends on the rule of shift and algorithm. By using AND gates the partial products can be produced and their summation can be performed by utilizing Full and Half Adders. All the operation in the n x n array multiplier are performed by utilizing Half Adders and n x (n-2) Full Adders. The bit array is designed by using the pipelined structure. Delay of the bit array multiplier equal to the width of the multiplier and speed of response will be reduced for wide fan-in multipliers.

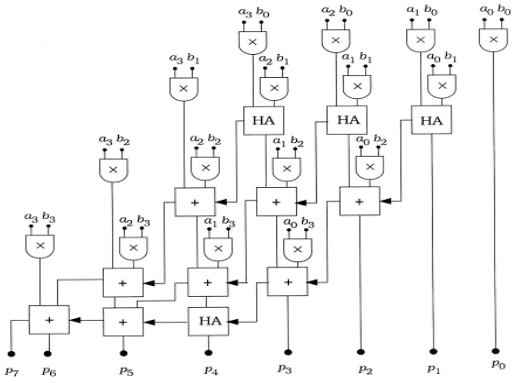

Figure 2: 4 Bit Array Multiplier

B. 8-Bit Ripple Carry Adder :

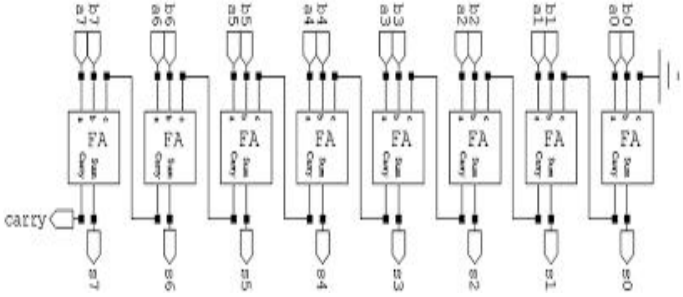

Figure 3: 8-Bit Ripple Carry adder

A Full adder describes that takes two input bits, a carry-in bit and produces the output sum and carry out. One type of reversible full adder is discussed and it is implemented with Peres gate. The 3x3 Peres Gate is singly worked as half adder circuit when third input is set to zero i.e. third input is treated as a constant input. To implement the Reversible full adder circuit using Peres gate it requires two Peres gates which should be arranged as shown in Fig 6. Now this entire circuit is denoted as name Peres Full Adder Gate (PFAG). Peres logic Full Adder Gate produces two garbage outputs (SJ1 and SJ2), and requires one constant input. The constant input is set to zero to obtain the desire outputs.

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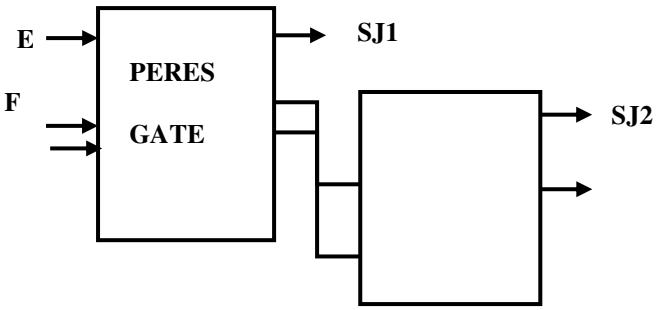

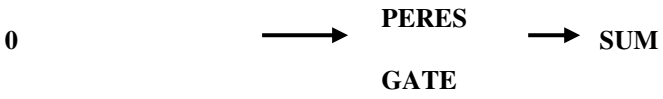

Fig. 12. Peres Gates as Reversible Full Adder

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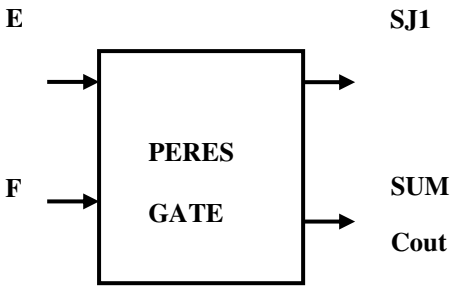

Fig. 13. Peres Gates as Reversible Half Adder

V. SIMULATION RESULT

The simulation Results discussed MAC design by using 4X4 Array Multiplier and 8-Bit Ripple carry Adder in reversible logic gate like Peres gate are modelled using VHDL module. The practical verification is done and synthesized in Xilinx ISE.

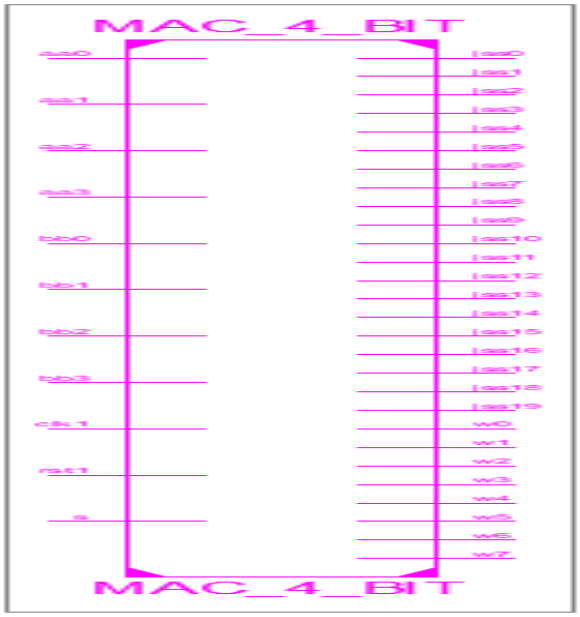

Figure 4: RTL Schematic of 4-Bit MAC

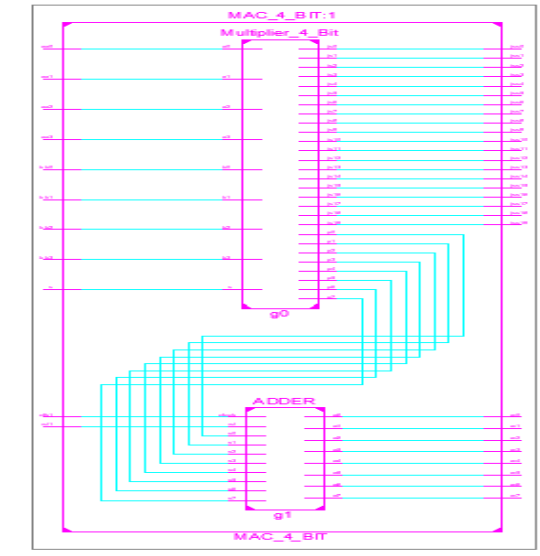

Figure 5:. RTL Schematic of 4-Bit MAC

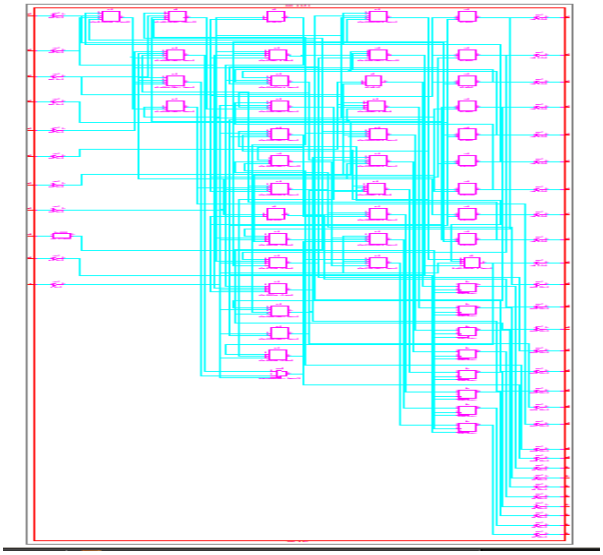

Figure 6: Technology View of 4-Bit MAC

Figure 7: Output Waveform of 8-Bit MAC

TABLE 1
PROPAGATION DELAY AND AREA COMPARISON

Peres Gate based MAC	No.of Slices	No.of LUT's	No.of Bounded I/O's	Delay
4-Bit MAC	29	42	27	31.64ns

V. CONCLUSIONS

4-Bit MAC was designed by using Reversible Logic 4x4 Array Multiplier and Reversible Logic 8-Bit Ripple Carry adder based on the Peres Logic. The performance of 4-Bit MAC architecture can be improved using reversible logic and evaluate the number of gate count, garbage output, quantum cost and delay of the 4-Bit MAC implemented using Reversible logic operation by using Peres Gate.

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