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Performance in Denser Networks Using IoT Adaptive Configurations

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ABSTRACT

Large-scale Internet of Things deployments demand long-range wireless communications, especially in urban and metropolitan areas. LoRa is one of the most promising technologies in this context due to its simplicity and flexibility. Indeed, deploying LoRa networks in dense Internet of Things scenarios must achieve two main goals i.e., efficient communications among many devices and resilience against dynamic channel conditions due to demanding environmental settings like the presence of many buildings. The project work investigates adaptive mechanisms to configure the communication parameters of LoRa networks in dense IoT scenarios and developed an open-source framework for end-to-end LoRa simulations. We then implement and evaluate LoRa to dynamically manage link parameters for scalable and efficient network operations. Our proposed solution significantly increases both the reliability and the energy efficiency of communications over a channel, almost irrespective of the network size. To show that the delivery ratio of very dense networks can be further improved by using a network-aware approach, wherein the link parameters are configured based on the global knowledge of the network.

Keywords: Embedded systems; IoT; LoRa; LoRaWAN.

1. Introduction

An embedded system is one kind of a computer system mainly designed to perform several tasks like to access, process, store and control the data in various electronics-based systems. One of its most important characteristics of these systems is, it gives the output within the time limits. Embedded systems support to make the work more perfect and convenient. So, we frequently use embedded systems in simple and complex devices too.Modern embedded systems are often based on microcontrollers (i.e. microprocessors with integrated memory and peripheral interfaces), but ordinary microprocessors (using external chips for memory and peripheral interface circuits) are also common, especially in more complex systems. In either case, the processors used may be types ranging from general purpose to those specialized in a certain class of computations, or even custom designed for the application at hand. A common standard class of dedicated processors is the digital signal processor (DSP).

Since the embedded system is dedicated to specific tasks, design engineers can optimize it to reduce the size and cost of the product and increase the reliability and performance. Some embedded systems are mass-produced, benefiting from economies of scale.One of the very first recognizably modern embedded systems was the Apollo Guidance Computer,[citation needed] developed ca. 1965 by Charles Stark Draper at the MIT Instrumentation Laboratory. At the project's inception, the Apollo guidance computer was considered the riskiest item in the Apollo project as it employed the then newly developed monolithic integrated circuits to reduce the size and weight. An early mass-produced embedded system was the Autonetics D-17 guidance computer for the Minuteman missile, released in 1961. When the Minuteman II went into production in 1966, the D-17 was replaced with a new computer that was the first high-volume use of integrated circuits.

Since these early applications in the 1960s, embedded systems have come down in price and there has been a dramatic rise in processing power and functionality. An early microprocessor for example, the Intel 4004 (released in 1971), was designed for calculators and other small systems but still required external memory and support chips. In 1978 National Engineering Manufacturers Association released a "standard" for programmable microcontrollers, including almost any computer-based controllers, such as single board computers, numerical, and event-based controllers.As the cost of microprocessors and microcontrollers fell it became feasible to replace expensive knob-based analog components such as potentiometers and variable capacitors with up/down buttons or knobs read out by a microprocessor even in consumer products. By the early 1980s, memory, input and output system components had been integrated into the same chip as the processor forming a microcontroller. Microcontrollers find applications where a general-purpose computer would be too costly.A comparatively low-cost microcontroller may be programmed to fulfill the same role as a large number of separate components. Although in this context an embedded system is usually more complex than a traditional solution, most of the complexity is contained within the microcontroller itself. Very few additional components may be needed and most of the design effort is in the software. Software prototype and test can be quicker compared with the design and construction of a new circuit not using an embedded processor.

1.1 EMBEDDED SYSTEMS TECHNOLOGIES:

Artificial Intelligence:

Artificial Intelligence creates intelligent in machines and it is a branch of computer science. Recent days it is an essential part of the technology Industry. It acts like humans when they have abundant information relating to the world. AI can be defined as the enabling of a machine to perform the logical analysis, obtain knowledge and adapt to an environment that varies. This technology is already being used in many applications such as self-driving cars, chatbots, personal voice assistant and super smart computing intensive.

Moreover, Artificial Intelligence is building intelligent systems with decision-making abilities. However, AI requires the use of hardware components to build truly intelligent machines. This is exactly where the relation between AI and embedded systems becomes so essential. The truth about Artificial Intelligence is more complex than it seems.

Virtual Reality and Augmented Reality:

Virtual Reality technology in an embedded system that allows the user to interact with an environment that exists in a computer. Virtual reality is a way to generate realistic images, sound, and other sensations. VR with higher resolution will challenge available display and processor technology. On the other hand, augmented reality is the latest innovations in the electronics industry. Augmented Reality adds virtual stuff to the real-world environment. These both technologies will become a big part of our world.

Deep Learning:

It represents a rich and yet unexplored embedded systems market that has a range of applications from image processing to audio analysis. Even though, the developers are mainly focused on cloud connectivity and security. It is emerging as the latest trend in an embedded system.

Embedded Security:

With the rise of the Internet of Things, the focus of developers and manufacturers is on security. The advanced technologies for embedded security will emerge as crucial generators for identifying devices in an IoT network, and as microcontroller security solutions that isolate security operations from normal operations.

Cloud Connectivity:

Getting embedded systems connected to the internet and cloud can take weeks and months in the traditional development cycle. Consequently, cloud connectivity technology is an important future market for embedded systems. These technologies are designed to simplify the process of connecting embedded systems with cloud-based services by reducing the underlying hardware complexities.

Each of the embedded systems is unique, and the hardware is highly specialized in the application domain. In the final analysis, "Things are beginning to move very quickly in the embedded space," and each advancement paves an exciting road to the times ahead.

1.2 ELEMENTS OF EMBEDDED SYSTEM

Software Components

Once the hardware is completed we need to build the software for the embedded devices. There are different software tools for programming and coding. These software tools are referred to as software components.

We need a program written in assembly or in embedded C language, then we compile it. This compiled code converted into HEX code. This hex code is programmed or burned into the ROM of the system using some programmer.

These are the tools that are generally used in embedded system development

Assembler

When you program in assembly language. This assembly language program is converted into the HEX code using this utility. Then using some hardware called as a programmer we write the chip.

Emulator

An emulator is hardware or software tool that has a similar functionality to the target system or guest system. It enables the host system to execute the functionality and other components. It is a replica of the target system. And used for debugging the code and issues.

Once program or code is fixed at the host system. It is transferred to the target system.

Debugger

Sometimes we are not getting expected results or output due to errors or bug. There are certain tools that are specifically used for the debugging process. Where we can see the controls flow and register value to identify the issue.

Compiler

A compiler is a software tool that converts one programming language into target code that a machine can understand. The compiler basically used for translating the highlevel language into the low-level language like machine code, assembly language or object code.

1.3 DESIGN OF EMBEDDED SYSTEMS:

A system designed with the embedding of hardware and software together for a specific function with a larger area is embedded system design. In embedded system design, a microcontroller plays a vital role. Micro-controller is based on Harvard architecture, it is an important component of an embedded system. External processor, internal memory and i/o components are interfaced with the microcontroller. It occupies less area, less power consumption.

There are two types of embedded systems microprocessors and micro-controller. Micro-processor is based on Von Neumann model/architecture (where program + data resides in the same memory location), it is an important part of the computer system, where external processors and peripherals are interfaced to it. It occupies more area and has more power consumption. The application of the microprocessor is personal computers.

Microcontrollers comprise the main elements of a small computer system on a single chip. They contain the memory, and IO as well as the CPU one the same chip. This considerably reduces the size, making them ideal for small embedded systems

Different steps in the embedded system design flow are as shown below:

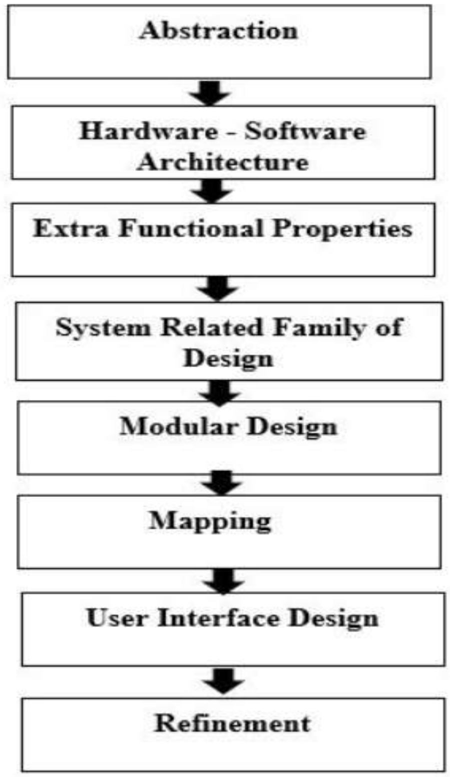


Fig. 1. Embedded system design flow

2. LITERATURE SURVEY

LoRa modulation is based on spread spectrum techniques and a variation of the chirp spread spectrum (CSS) with integrated forward error correction (FEC). It operates in the lower Industrial, Scientific, and Medical (ISM) bandwidths (USA: 915MHz, EU: 433MHz and 868MHz). The LoRa modulation can be utilized by many different protocol architectures such as Star, Mesh, and 6lowPAN. The LoRa Alliance has standardized the MAC protocol called LoRaWAN. LoRaWAN defines the communication protocol and system architecture for the network while the LoRa physical layer enables the long-range communication link. The edge nodes of the LoRaWAN network can transfer data to multiple base stations. LoRaWAN is an open standard governed by the LoRa Alliance. In this regard, the works that we have surveyed describe the different types of network's and techniques, how they actually have served the purpose and the primary difference between our project and those literatures that we have contemplated.

LoRa technology was compared exhaustively with other LPWAN technologies in terms of architecture, battery lifetime, network capacity, device classes, and security, where the LoRaWAN protocol is 3 to 5-fold more advantageous than Sigfox, NB-IoT, and LTE-M. In a more explicit survey, provides a comparative analysis on LoRa and NB-IoT, claiming that there is no LPWAN technology that fits all requirements, but both LoRa and NB-IoT could be advantageous based on their appropriateness to the system requirements and features they could offer. This analysis shows that unlicensed LoRa has advantages about the battery lifetime, capacity, and cost while the licensed NB-IoT offers advantages in terms of Quality of Service (QoS), latency, reliability, and range.

We found that LoRa has great potential for deployment in a physical environment both indoors and outdoors, whether as the interface for sensor nodes or the gateway. The results of this survey prove the universal application prospects of LoRa. Applications are diverse, ranging from monitoring in healthcare, tracking, environmental monitoring, to structural health monitoring.This paper focuses on Adaptive Data Rate (ADR) mechanism built in LoRa to dynamically manage link parameters for scalable and efficient network operations. Extensive simulations show that ADR is effective in increasing the network delivery ratio under stable channel conditions, while keeping the energy consumption low.

The paper [2] contemplates on the emerging transmission technologies dedicated to IoT networks [2]. Characteristics of LoRa are based on three basic parameters: Code Rate (CR), Spreading Factor (SF) and Bandwidth (BW). This paper provides in depth analysis of the impact of these three parameters on the data rate and time on air.

The paper [3] focused on the performance of LoRa when it is used on campus. the LoRa transmission performance from LoRa end-devices to the LoRa gateway how packet losses were affected by the distance between the end-device and the gateway, the transmit power, the payload length, the antenna angle, the time of day, and the weather conditions. The pattern of LoRa packet losses were also measured.

The paper [4] focuses on LoRaWAN operations focused on performance evaluation of its channel access as the most crucial component for massive machine type communication and to improve LoRaWAN performance.

3. Existing Method & Proposed method

3.1 Block Diagram Of Existing System

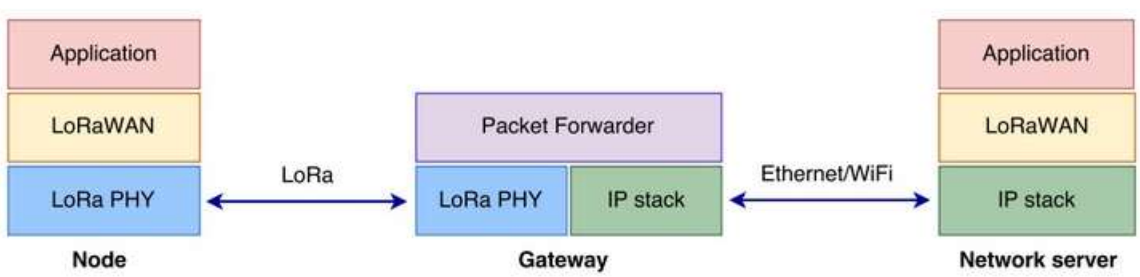


Fig. 2: Block Diagram Of LoRa Network

3.2 DESCRIPTION:

LoRa (Long Range) is a low-power wide-area network (LPWAN) technology. It is based on spread spectrum modulation techniques derived from chirp spread spectrum (CSS) technology. It was developed by Cycleo of Grenoble, France and acquired by Semtech the founding member of the LoRa Alliance. LoRa uses license-free sub-gigahertz radio frequency bands like 433 MHz, 868 MHz (Europe), 915 MHz (Australia and North America) and 923 MHz (Asia). LoRa enables long-range transmissions (more than 10 km in rural areas) with low power consumption.The technology covers the physical layer, while other technologies and protocols such as LoRaWAN (Long Range Wide Area Network) cover the upper layers. In January 2018, new LoRa chipsets were announced, with reduced power consumption, increased transmission power, and reduced size compared to older generation.

3.3 Block Diagram Description of Existing System

LoRa devices have geolocation capabilities used for trilaterating positions of devices via timestamps from gateways. LoRa and LoRaWAN permit long-range connectivity for Internet of Things (IoT) devices in different types of industries. LoRa uses a proprietary spread spectrum modulation that is similar to and a derivative of Chirp spread spectrum (CSS) modulation. The spread spectrum LoRa modulation is performed by representing each bit of payload information by multiple chirps of information. The rate at which the spread information is sent is referred to as the symbol rate, the ratio between the nominal symbol rate and chirp rate is the spreading factor (SF) and represents the number of symbols sent per bit of information. LoRa can trade off data rate for sensitivity with a fixed channel bandwidth by selecting the amount of spread used (a selectable radio parameter from 7 to 12). Lower SF means more chirps are sent per second; hence, you can encode more data per second. Higher SF implies fewer chirps per second; hence, there are fewer data to encode per second. Compared to lower SF, sending the same amount of data with higher SF needs more transmission time, known as airtime. More airtime means that the modem is up and running longer and consuming more energy. The benefit of high SF is that more extended airtime gives the receiver more opportunities to sample the signal power which results in better sensitivity.

In addition, LoRa uses Forward Error Correction coding to improve resilience against interference. LoRa's high range is characterized by high wireless link budgets of around 155 dB to 170 dB.

LoRaWAN:

Since LoRa defines the lower physical layer, the upper networking layers were lacking. LoRaWAN is one of several protocols that were developed to define the upper layers of the network. LoRaWAN is a cloud-based medium access control (MAC) layer protocol but acts mainly as a network layer protocol for managing communication between LPWAN gateways and end-node devices as a routing protocol, maintained by the LoRa Alliance.

LoRaWAN defines the communication protocol and system architecture for the network, while the LoRa physical layer enables the long-range communication link. LoRaWAN is also responsible for managing the communication frequencies, data rate, and power for all devices. Devices in the network are asynchronous and transmit when they have data available to send. Data transmitted by an end-node device is received by multiple gateways, which forward the data packets to a centralized network server. The network server filters duplicate packets, performs security checks, and manages the network.Data is then forwarded to application servers. The technology shows high reliability for the moderate load; however, it has some performance issues related to sending acknowledgements.

LoRa Alliance

The LoRa Alliance is a 501(c) association created in 2015 to support LoRaWAN (long range wide-area network) protocol as well as ensure interoperability of all LoRaWAN products and technologies. This open, nonprofit association has over 500 members. Some members of the LoRa Alliance IBM, Actility, MicroChip, Orange, Cisco, KPN, Swisscom, Semtech, A2A Smart City SPA, Bouygues Telecom, Singtel, Proximus and Cavagna Group.

In 2018, the LoRa Alliance had over 100 LoRaWAN network operators in over 100 countries. The Alliance is administered by the VTM Group in Beaverton, Oregon. Geoff Mulligan was its chairman until 2018, when Donna Moore became the CEO and chairwoman.

Semtech's LoRa chips transmit in the sub-gigahertz spectrum (109MHz, 433MHz, 866MHz, 915MHz), which is an unlicensed band that has less interference than others (like the 2.4 GHz range used by Wi-Fi, Bluetooth, and other protocols). At those frequencies, signals penetrate obstacles and travel long distances while drawing relatively little power ideal for many IoT devices, which are often constrained by battery life.

Within the sub-GHz spectrum, LoRa chips use a spread-spectrum strategy to transmit at a variety of frequencies and data rates. That allows the gateway to adapt to changing conditions and optimize the way it exchanges data with each device.

Semtech produces transceiver chips for devices to be connected (nodes), and gateways to connect them. A single gateway can communicate with several hundred thousand nodes up to 2 miles away in unobstructed environments, and even in a city can penetrate buildings to achieve a range of several miles. End-nodes can remain operational for a supposed 10 years running on two AAA batteries (drawing 10mA for the receiver, under 200nA in sleep mode).

3.4 Proposed System :

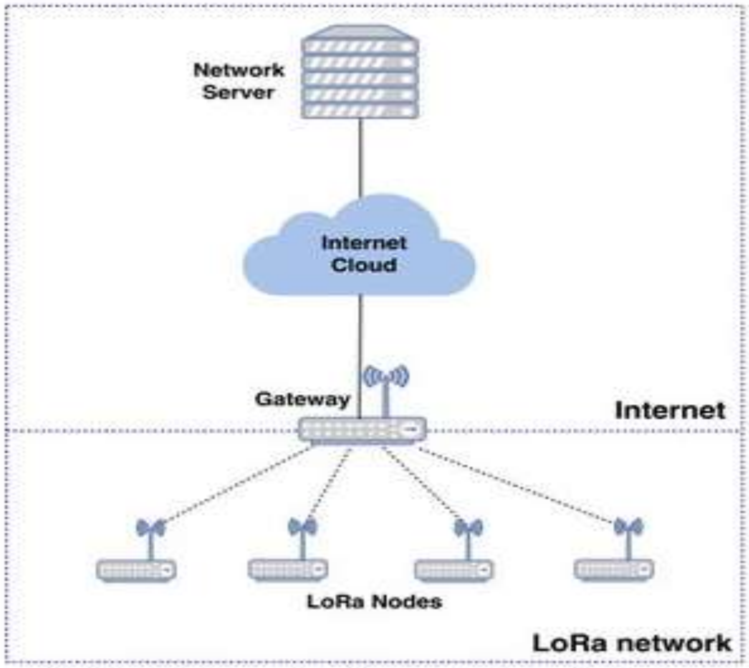


Fig. 3. Proposed Network

This Project is Developed and tested on the Dev-C++ Software ,The Network is an open and community-driven Internet of Things (IoT) network. However, the management of LoRa networks for IoT deployments faces several challenges, in-cluding: a large and highly-varying number of nodes; diverse wireless scenarios characterized by demanding environmental factors (e.g., dense urban settings with many buildings); interference due to other co-located networks operating on the same unlicensed frequency bands.

These challenges may compromise scalability, eventually affecting the reliability of services running on top of IoT deployments One option to address such challenges is to dynamically adapt the operating parameters of wireless communications in the network. Although many recent works have characterized the communication performance of LoRa networks, they have not thoroughly investigated the impact of dynamic management of communication parameters. Indeed, this article targets adaptive configuration of LoRa networks for scalable IoT deployments. Such an adaptive configuration can be achieved with either a link-based or a network-aware approach. Link-based schemes configure the communication parameters inde-pendently for each wireless link between nodes.

On the other hand, network-aware approaches adapt these parameters for a certain link by leveraging a global knowledge of the nodes in the network. In this regard, our work evaluates both approaches to configure the transmission parameters at the physical layer of LoRa to improve both reliability and energy efficiency in dense IoT scenarios. Performance of ADR is severely affected by a highly-varying wireless channel. The delivery ratio of very dense networks can be further improved by using a network-aware approach, wherein the link parameters are configured based on the global knowledge of the network (e.g., the location of the devices). A LoRa network relies on two components, namely, LoRa and LoRaWAN, each corresponding to a different layer of the protocol stack. LoRa itself is a proprietary physical layer developed by Semtech Corporation. LoRaWAN, on the other hand, is described in an open specification developed by the LoRa Alliance. LoRaWAN constitutes the medium access control (MAC) and network layers in LoRa networks. The LoRa physical layer enables long-distance, low-power communication and operates in the unlicensed sub-GHz ISM band. LoRa utilizes chirp spread spectrum modulation to encode an input signal into chirp pulses spread over a wide spectrum. This technique enables long-distance communication, even though this results in a low data rate. Each LoRa transmission is characterized by five parameters: spreading factor, transmission power, code rate, center frequency and bandwidth. These parameters affect the communication range, the data rate, the robustness to interference or noise, and the ability of a receiver to decode the signal. The available values for each parameter depend on the region where LoRa devices are deployed. The spreading factor is the ratio between the data symbol rate and chirp rate. The configuration of the spreading factor allows tuning the data rate and the reachable distance. In fact, the data rate is lower at higher spreading factors, but the communication range is higher. Choosing different spreading factors also enables orthogonal signals, implying that a receiver can successfully receive distinct signals sent over a given channel at the same time. The transmission power can be configured based on the region and the bandwidth used for transmissions. The code rate is the forward error correction rate, and it affects the airtime of packet transmissions. The center frequency depends on the ISM band used in a particular region. Finally, the bandwidth influences the data rate of transmissions. The LoRaWAN specification defines an open standard for the network protocols and the system architecture of LoRa networks. LoRaWAN relies on an ALOHA-based MAC protocol , which reduces the complexity of end-devices.The network architecture consists of a hierarchical topology, wherein LoRa nodes communicate with gateways over the LoRa physical layer. A node is not associated with a particular gateway; instead, all gateways within the range of a transmitter can receive messages. The gateways simply relay received messages to a central network server. The communication between gateways and the network server takes place over the standard Internet Protocol (IP). The central network server manages the network by processing the incoming messages, filtering duplicate packets, forwarding messages to application servers, and sending responses to nodes through a single designated gateway.

MAC protocol as well as network elements including gateways and network servers. Moreover, FLoRa includes a module to characterize the energy consumption of LoRa end devices. This section details the implementation of FLoRa. We first describe the characterization of the LoRa physical layer, then discuss the adopted energy model. We also present the key features of the network elements and the architecture supported by the simulator. A. LoRa Links FLoRa allows to configure all the transmission parameters in the LoRa physical layer: spreading factor, center frequency, bandwidth, code rate, and transmission power. These parameters determine the communication range and the occurrence of collisions. In particular, a LoRa transmission is successful if the received power is greater than the receiver sensitivity. The received power depends on the transmission power and the losses due to signal attenuation and shadowing. This is modeled using the well-known log-distance path loss model with shadowing, which calculates the path loss based on the distance between the transmitter and receiver. FLoRa supports both urban and suburban environments. A successful transmission also depends on whether LoRa transmissions interfere with each other or not. To this end, we use the collision model. The main assumption is that two transmissions in orthogonal channels (for instance, transmissions with different spreading factors) do not collide. If two messages are in non-orthogonal channels, a collision occurs when they overlap in time. Furthermore, the collision model includes the capture effect. Accordingly, the stronger of two colliding signals is decoded, provided that the power difference between the signals is more than 6 dBm and at least 5 symbols in the preamble are detected.

The energy expenditure is modeled by a state-based energy consumer module, wherein the energy consumed depends on the amount of time spent by the LoRa radio in a particular state. The three main states of a LoRa radio are transmit,receive and sleep. The radio is switched to sleep mode after transmitting or receiving a frame. The energy consumed in the transmit state depends on the transmission power level. The values of the instantaneous current for each transmission power level are obtained. The current drawn during the receive and sleep modes are derived from the Semtech SX1272/73 datasheet with a supply voltage of 3.3 V.LoRa enables end-to-end network simulations by modeling LoRa nodes, gateways and network servers. The gateway is able to receive LoRa transmissions from nodes on multiple channels simultaneously, in compliance with the LoRaWAN specifications. The gateway and the network server communicate over IP. The physical layer between the gateway and the network server can be realized with existing INET modules such as Ethernet and WiFi links. Similarly, delays in the backhaul network can be described by an appropriate configuration of the relevant link parameters. A network can contain multiple gateways; the network server filters out duplicate packets from multiple gateways and sends downlink data to a node through the gateway with the highest link quality indicator. The network server also implements the management algorithms described in the next section.

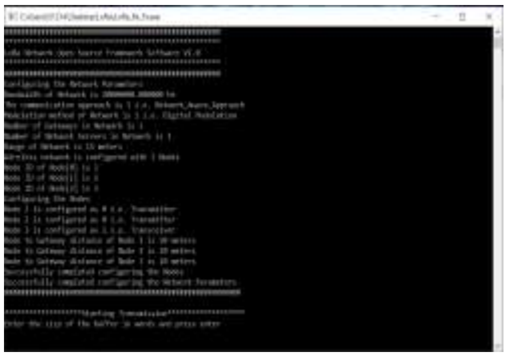
LoRa networks are expected to support a large number of devices exchanging data over the LoRa physical layer. Managing the transmission parameters of the physical layer plays an important role in determining the capacity and scalability of LoRa networks. To this end, the LoRaWAN specification describes a link-based Adaptive Data Rate (ADR) mechanism, which dynamically modifies the transmission parameters for links between nodes and gateways. This section first describes the features of ADR. We then propose an improved version of the ADR scheme to achieve better performance under variable channel conditions. Finally, we describe a network-aware approach, wherein a global knowledge on the network is used to adapt the transmission parameters.

ADR is designed to efficiently set the data rate and the transmission power of static nodes with two main goals: increase the overall capacity of the network and maximize the battery life of the nodes. ADR achieves this by estimating a link budget, which is the sum of all gains and losses in each wireless link between a node and a gateway. For instance, a node located close to a gateway can transmit data with a low spreading factor so as to lower the message transmission time. This allows other nodes to utilize the available channel for other transmissions. Battery life is increased by dynamically assigning the transmission power of a node based on its distance to the gateway. The ADR mechanism runs asynchronously at the LoRa node and at the network server. Most of the complexity in ADR is assigned to the network server, with the goal to keep the nodes as simple as possibleits main goal is to increase the SF (thereby reducing the data rate) if uplink transmissions cannot reach the gateway. If a downlink frame is not received within a configurable number of frames, the node increases the SF of the subsequent uplink frame. This increases the transmission range and, thus, also the probability of reaching a gateway.The part of ADR running at the network server 2, referred to as ADR-NET, is described , thisallows the network server to change the TP and the SF for the uplink data transmissions of end nodes. To this end, the network server estimates the link budget of each node by using the SNR of received frames. The transmission parameters are then estimated based on the knowledge of the minimum SNR (SNRreq) required for demodulation. We refer to the version of ADR running at the network server according to the implementation in the Things Network, which is based on the reference (yet not publicly-available) rate adaptation algorithm by Semtech. The newly calculated parameters are communicated to the LoRa node through a downlink frame. The node uses the new parameters for future transmissions until otherwise instructed. Note that the network server does not increase the SF (i.e., it does not reduce the data rate), asthis is done by the LoRa node through ADR-NODE.

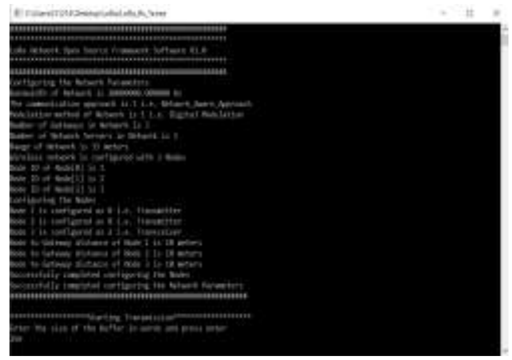
The ADR-NET estimates the link quality by using the maximum SNR value from historical samples. This choice is ideal when there is no variability in the channel quality. However, taking the maximum value is an optimistic approach to estimate link quality when the physical channel conditions are variable, for instance, due to weather or moving obstaclesbetween two communicating devices. The previously described ADR algorithms adapt the transmission parameters of each node based on an estimated link budget. However, the performance of a LoRa network depends not only on such a budget but also on the occurrence of other simultaneous transmissions with the same spreading factor. This is determined by the spatial configuration of the deployed LoRa devices, namely, by the actual locations of both gateways and nodes. Indeed, it is possible to efficiently assign spreading factors to nodes when the location of all devices in the network. Accordingly, we calculate the optimal distribution of spreading factors that balances the collision probabilities between different spreading factors in the whole network. The probability of collisions in each spreading factor follows the unslotted ALOHA model. The optimal spreading factor distribution is obtained with a genetic algorithm. Once the distribution of spreading factors is known, our network-aware approach configures the parameters as follows. We first sort the nodes according to increasing distance from the gateway. We then assign spreading factors to each node according to the optimal distribution: nodes closer to the gateway are assigned a lower spreading factor and those further away a higher spreading factor.

5. RESULTS

"LoRa_Rx_Tx.exe" application opens as shown in the figure (a). In the figure (a) shown, we can see that the Network is configured with 3 nodes and the Network parameters like type of modulation, communication approach, number of network servers, range of network, gateway to node distance, etc are configured. As shown in the figure (b), enter the size of the buffer. The buffer size is used to specify the amount of data that is going to be transmitted from a specific Node. After, entering the buffer size, press enter key. The buffer size is displayed on the terminal as shown in the image (c). Next, a message to enter the data, that is to be transmitted from Node0 to the Gateway is displayed on the terminal as shown in the below image:

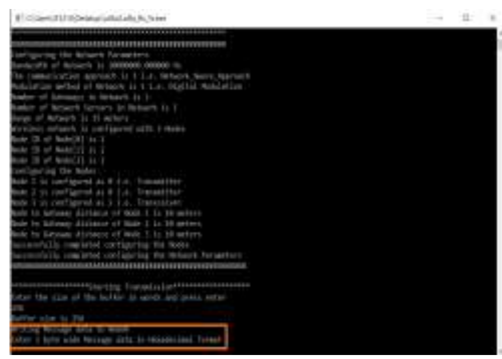


(a)



(b)

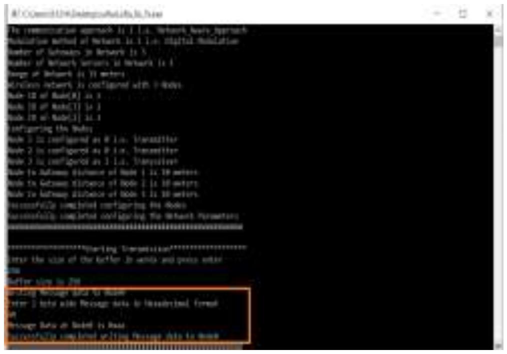
(c)

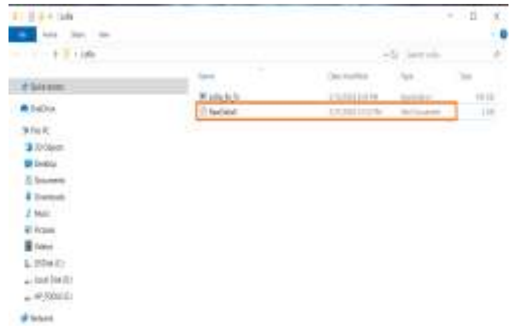


(d)

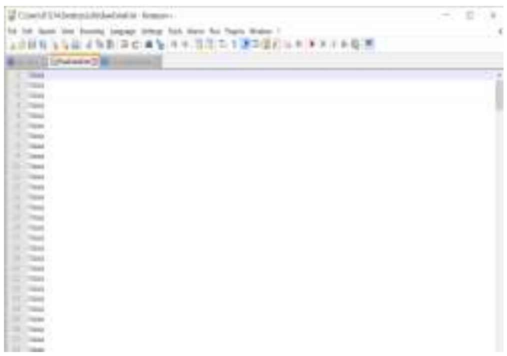
Fig. 4. Network configuration: Part I.

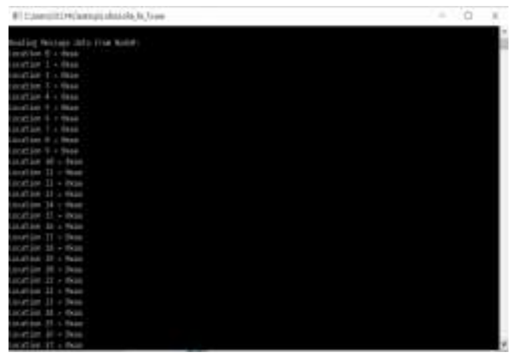
Enter the message data and press enter as shown in the below image (a). When the message data is entered a file is created in the "LoRa" directory on the desktop as shown in the below image (b) and the data is written to the file. When the RawData0 file is opened, you can see the data "AA" written to all the 256 locations as shown below (c). The message data is successfully written to Node0 and the data is read back as shown in the below image (d).





(a) (b)



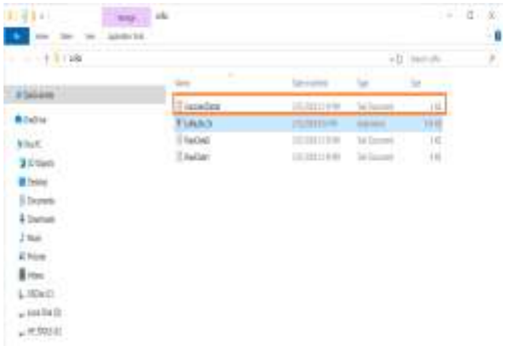


(c) (d)

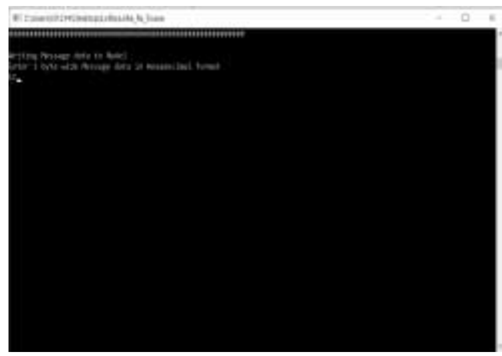
Fig. 5. Network configuration: Part II.

Now, the message data 0xAA is encrypted before transmitting to Gateway1 as in figure (a). The encoded data at Node0 is written to a file “EncodedData0.txt” in the “LoRa” directory on the desktop. Open the “EncodedData0.txt” file to check the encoded data as in figure (b). Encoded data is written to the file. The data is successfully encoded and read back as shown in the below image (c).

Encoded Data = Message Data ^ Carrier Data.
Where, Message Data = 0xAA, Carrier Data = 0x55
0xAA ^ 0x55 = 0xFF
Hence, Encoded Data = 0xFF.
Similarly, enter the data for Node1 as in figure (d).



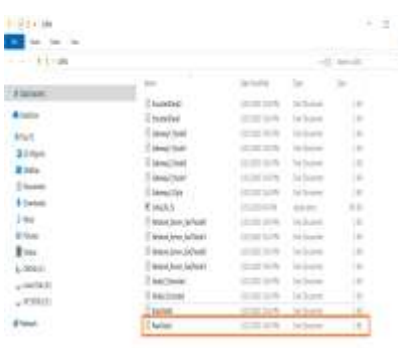
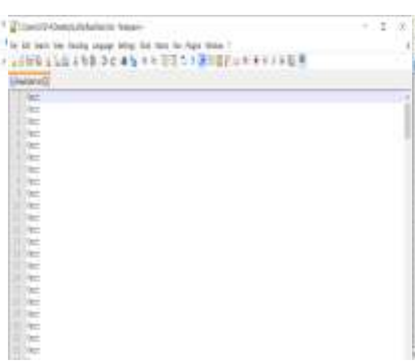
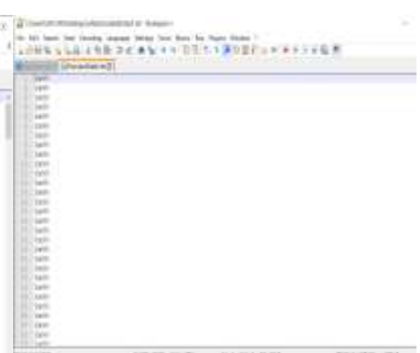

(a) (b)

(c) (d)

Fig. 6. Network configuration: Part III.

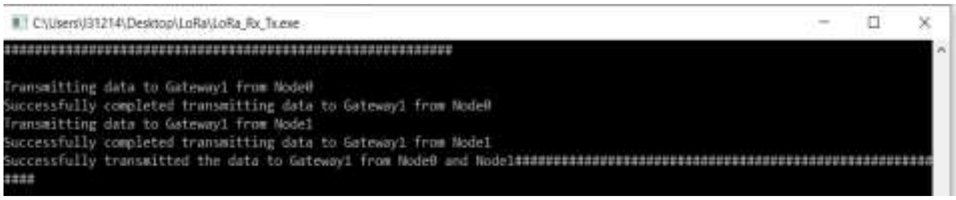
When the message data for Node1 is entered a file is created with the name “RawData1” and the message data is written to the file as shown in the below image (a). When the “RawData1” file is opened, you can see the message data “0xCC” written to all the 256 locations as shown in the below image (b). Similarly, as done at Node0, the data at Node1 is encoded before transmitting the data to Node1 (c).The encoded data at Node1 is as shown in the below image:

(a) (b) (c)

Fig. 7. Network configuration: Part IV.

The encoded data from Node0 and Node 1 are transmitted to both Gateway1 and Gateway2as shown in the below images:



(a)

(b)

Fig. 8. Network configuration: Part V.

The data at Gateway1 and Gateway2 are written to the files "Gateway1_Node0.txt", "Gateway1_Node1", "Gateway2_Node0" and "Gateway2_Node1" in the "LoRa" directory on the desktop:

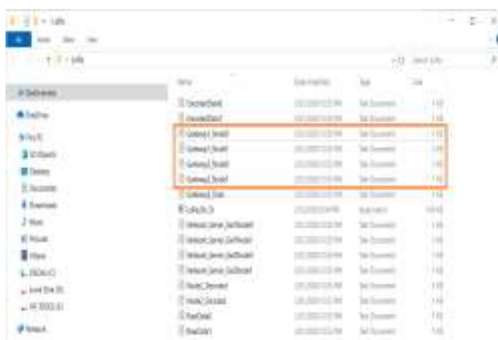


Fig. 9. Gateway setup.

Later data from Gateway1 and Gateway2 is transmitted to the Network server as shown in the below image:

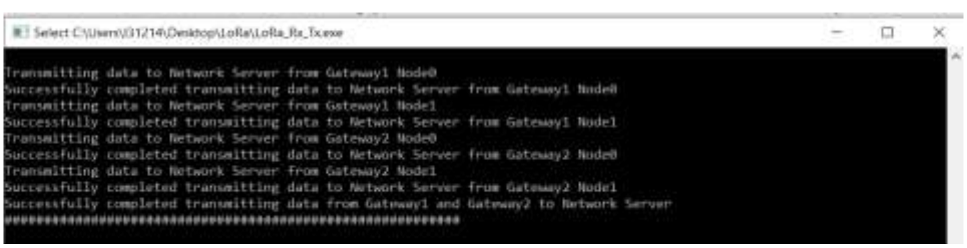


Fig. 10. Gateway configuration part I.

The data at Network server are written to the files "Network_Server_Gw1Node0.txt", "Network_Server_Gw1Node1.txt", "Network_Server_Gw2Node0.txt" and "Network_Server_Gw2Node1.txt" in the "LoRa" directory on the desktop:

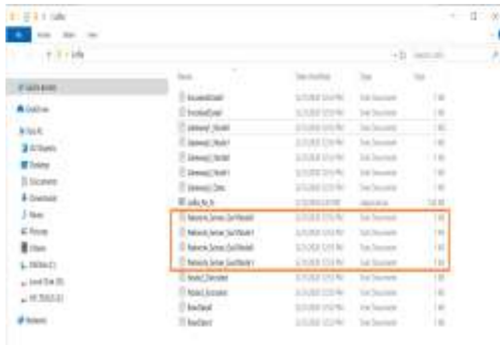
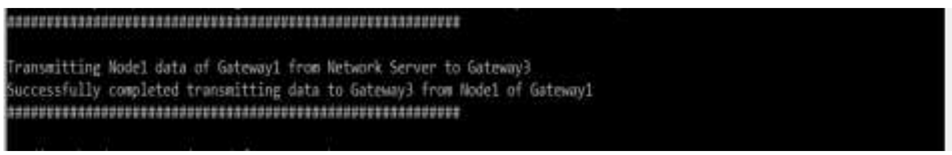


Fig. 11. Gateway configuration part II.

Now, the data from Network server is transmitted to Gateway3 as shown in the below image:



The data at Gateway3 is written to the file "Gateway3_Data.txt" in the "LoRa" directory on the desktop:

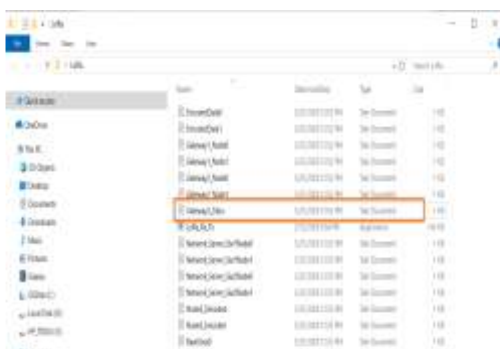


Fig. 12. Gateway configuration part III.

Next, the data from Gateway3 is transmitted to Node2 as shown below:

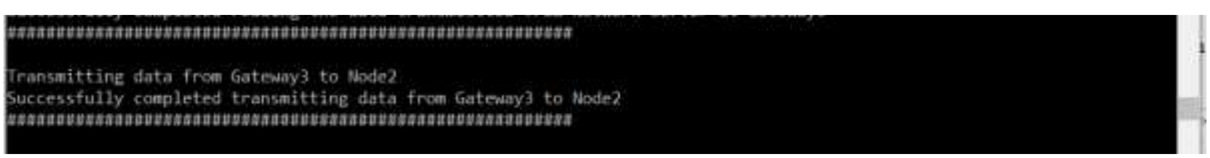


Fig. 13. Gateway configuration part IV.

The Data at Node2 is the encoded data from Node1, the data at Node2 is written to the file “Node2_Encoded.txt” in the “LoRa” directory on the desktop:

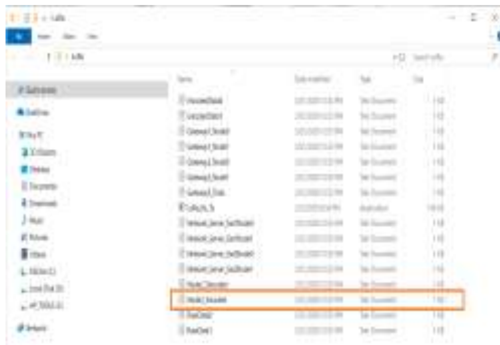


Fig. 14. Gateway configuration part V.

Now, the data at Node2 is decoded, as shown below:

Fig. 15. Node decoding.

The decoded data at Node2 is written to the file “Node2_Decoded.txt” in the “LoRa” directory on the desktop:

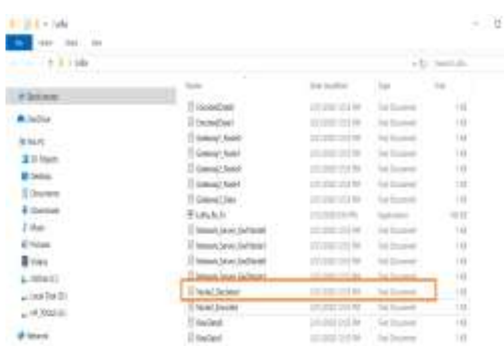
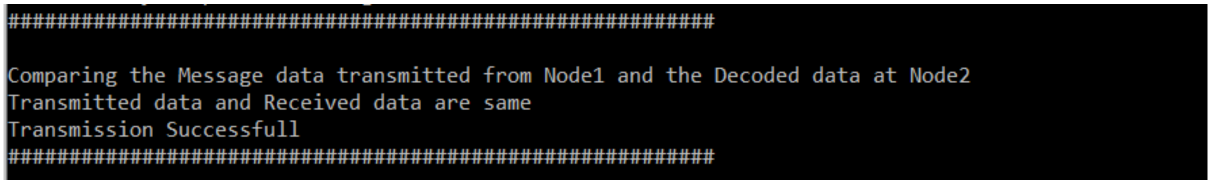


Fig. 16. Node configuration.

Now, the data transmitted from Node1 and the data received at Node2 are compared as shown in the below image:



As the the data transmitted and received are same, a message is displayed on the terminal stating that the transmission is successful.Below is the image of the message data from Node1 and Node2:

Fig. 17. Final outcome of the network configuration

The application areas of the proposed model are Reindeer tracking in Finland, Glasgow IoT network, IoT networks in Argentina, Brazil and Estonia, Smart fire alarms and fire detection, Smart Parking, Black rhino poaching protection and endangered sea turtle monitoring, Natural disaster prediction, Cotton farming in Australia, Utility metering in India, Autonomous irrigation and soil health monitoring, Smart water monitoring and water monitoring for commercial farms, City-wide network in Calgary, Alberta, Canada, IoT Network in Alba Iulia, Romania.

The main benefits of LoRa are low range, low power and low-cost connectivity. Another key feature of LoRa and LoRaWan is security for both devices and network, coverage, and energy efficiency.

6. CONCLUSION

Here, in this paper we have thoroughly analyzed the LORA networks and developed the software to configure them based on the user requirements. The results show how the LORA networks are configured and how the data is transmitted between them.

7. References

[1] Slabicki, Mariusz, Gopika Premsankar, and Mario Di Francesco, "Adaptive configuration of LoRa networks for dense IoT deployments," In NOMS 2018-2018 IEEE/IFIP Network Operations and Management Symposium, pp. 1-9. IEEE, 2018.

[2] Noreen, Umber, Ahcène Bounceur, and Laurent Clavier,"A study of LoRa low power and wide area network technology," In 2017 International Conference on Advanced Technologies for Signal and Image Processing (ATSIP), pp. 1-6. IEEE, 2017.

[3] Wang, Shie-Yuan, Yo-Ru Chen, Tzu-Yang Chen, Chia-Hung Chang, Yu-Hsiang Cheng, Chun-Chia Hsu, and Yi-Bing Lin,"Performance of LoRa-based IoT applications on campus," In 2017 IEEE 86th Vehicular Technology Conference (VTC-Fall), pp. 1-6. IEEE, 2017.

[4] Bankov, Dmitry, Evgeny Khorov, and Andrey Lyakhov, "On the limits of LoRaWAN channel access," In 2016 International Conference on Engineering and Telecommunication (EnT), pp. 10-14. IEEE, 2016.

[5] Semtech LoRa Technology. [Online]. Available at: https://www.semtech.com/lora

[6] Embedded Wireless: Low-Power Wide-Area Network. [Online]. Available at: https://www.microchip.com/design-centers/wireless-connectivity/low-power-wide-area-networks/lora-technology

[7] LoRawireless basics. . [Online]. Available at: https://www.electronicproducts.com/Digital_ICs/Communications_Interface/LoRa_wireless_basics.aspx

[8] Vallabhuni Vijay, P. Chandra Shekar, V. Siva Nagaraju, S. China Venkateswarlu, and Shaik Sadulla, "High Performance 2:1, 4:1 And 8:1 Binary And Ternary Multiplexer Realization Using CNTFET Technology," Journal of Critical Reviews, vol. 7, iss. 6, 2020, pp. 1159–1163.

[9] Kurra, Anil Kumar, and Usha Rani Nelakuditi, "A secure arbiter physical unclonable functions (PUFs) for device authentication and identification," Indonesian Journal of Electrical Engineering and Informatics (IJEEI), 7, no. 1, 2019, pp. 117–127.

[10] Vallabhuni Vijay, V. Siva Nagaraju, M. Sai Greeshma, B. Revanth Reddy, U. Suresh Kumar, and, C. Surekha, "A Simple and Enhanced Low-Light Image Enhancement Process Using Effective Illumination Mapping Approach," Lecture Notes in Computational Vision and Biomechanics, Cham, Switzerland. 2019, pp. 975–984.

[11] Kurra, A.K., and Sadulla, S., "Analysis of physical unclonable functions (PUFS) for secure key generation on smartcard chips," Journal of Advanced Research in Dynamical and Control Systems, 9, 2017, pp. 1735-1745.

[12] Vallabhuni Vijay, "Second Generation Differential Current Conveyor (DCCII) And Its Applications," Vignan's Foundation for Science, Technology & Research (Deemed to be University), Guntur, 2017.

[13] Rajeev Ratna Vallabhuni, J. Sravana, M. Saikumar, M. Sai Sriharsha, and D. Roja Rani, "An advanced computing architecture for binary to thermometer decoder using 18nm FinFET," 2020 Third International Conference on Smart Systems and Inventive Technology (ICSSIT), Tirunelveli, India, 20-22 August, 2020, pp. 510–515.

[14] P. Chandra Shaker, V. Parameswaran, M. Srikanth, V. Vijay, V. Siva Nagaraju, S.C. Venkateswarlu, Sadulla Shaik, and Vallabhuni Rajeev Ratna, "Realization and Comparative analysis of Thermometer code based 4-Bit Encoder using 18nm FinFET Technology for Analog to Digital Converters," Advanced Intelligent Systems and Computing (AISC), 2020.

[15] Mohammad Khadir, Kancharapu Chaitanya, S. Sushma, V. Preethi, and Vallabhuni Vijay, "Design Of Carry Select Adder Based On A Compact Carry Look Ahead Unit Using 18nm Finfet Technology," Journal of Critical Reviews, vol. 7, iss. 6, 2020, pp. 1164–1171.

[16] Rajeev Ratna Vallabhuni, D.V.L. Sravya, M. Sree Shalini, and G. Uma Maheshwararao, "Design of Comparator using 18nm FinFET Technology for Analog to Digital Converters," 2020 7th International Conference on Smart Structures and Systems (ICSSS), Chennai, India, 23-24 july, 2020, pp. 318–323.

[17] Shaik, Sadulla, Anil Kumar Kurra, and A. Surendar, "High secure buffer based physical unclonable functions (PUF's) for device authentication," Telkomnika, 17, no. 1, 2019.

[18] P. Saritha, J. Vinitha, S. Sravya, V. Vijay, and E. Mahesh, "4-Bit Vedic Multiplier with 18nm FinFET Technology," 2020 International Conference on Electronics and Sustainable Communication Systems (ICESC), Coimbatore, India, 2020, pp. 1079–1084.

[19] Vijay, V., J. Prathiba, S. Niranjan Reddy, and P. Praveen Kumar, "A REVIEW OF THE 0.09 µm STANDARD FULL ADDERS," International Journal of VLSI Design & Communication Systems, vol. 3, no. 3, 2012, p. 119.

[20] Kurra, Anil, and Usha Rani Nelakuditi, "Design of a Reliable Current Starved Inverter Based Arbiter Physical Unclonable Functions (PUFs) for Hardware Cryptography," Ingénierie des Systèmes d Inf., 24, no. 4, 2019, pp. 445–454.

[21] V. Vijay, and Avireni Srinivasulu, "Tunable Resistor and Grounded Capacitor Based Square Wave Generator Using CMOS DCCII," International J. Control Theory and Applications, vol. 8, 2015, pp. 1–11.

[22] Rajeev Ratna Vallabhuni, K.C. Koteswaramma, B. Sadgurbabu, and Gowthamireddy A, "Comparative Validation of SRAM Cells Designed using 18nm FinFET for Memory Storing Applications," Proceedings of the 2nd International Conference on IoT, Social, Mobile, Analytics & Cloud in Computational Vision & Bio-Engineering (ISMAC-CVB 2020), 2020, pp. 1-10.

[23] Vallabhuni Vijay, and Avireni Srinivasulu, "A low power waveform generator using DCCII with grounded capacitor," International Journal of Public Sector Performance Management, vol. 5, 2019, pp. 134–145.

[24] P. Chandrashekar, R. Karthik, O. Koteswara Sai Krishna, and Ardhi Bhavana, "Design of low threshold Full Adder cell using CNTFET," International Journal of Applied Engineering Research, vol. 12, no. 12, 2017, pp. 3411–3415.

[25] Vallabhuni Vijay, C. V. Sai Kumar Reddy, Chandrashaker Pittala, "System and Method to Improve Performance of Amplifiers Using Bias Current," The Patent Office Journal No. 43/2019, India. International classification: C12Q1/6869. Application No. 201941042648 A.

[26] V. Vijay, and Avireni Srinivasulu, "A square wave generator using single CMOS DCCII," in proceedings of the 2013 IEEE International SoC Design Conference (IEEE ISoCC-2013), Busan, South Korea, November 17-19, 2013, pp. 322–325.

[27] Rajeev Ratna Vallabhuni, G. Yamini, T. Vinitha, and S. Sanath Reddy, "Performance analysis: D-Latch modules designed using 18nm FinFET Technology," 2020 International Conference on Smart Electronics and Communication (ICOSEC), Tholurpatti, India, 10-12, September 2020, pp. 1171–1176.

[28] Vallabhuni Vijay, and Avireni Srinivasulu, "A Novel Square Wave Generator Using Second Generation Differential Current Conveyor," Arabian Journal for Science and Engineering, vol. 42, iss. 12, 2017, pp. 4983–4990.

[29] V. Vijay, J. Prathiba, S. Niranjan reddy, Ch. Srivalli, and B. Subbarami reddy, "Performance evaluation of the CMOS Full adders in TDK 90 nm Technology," International Journal of Systems, Algorithms & Applications, vol. 2, iss. 1, 2012, pp. 711.

[30] Rajeev Ratna Vallabhuni, S. Lakshmanachari, G. Avanthi, and Vallabhuni Vijay, "Smart Cart Shopping System with an RFID Interface for Human Assistance," 2020 3rd International Conference on Intelligent Sustainable Systems (ICISS), Palladam, India, December 4-5, 2020, pp. 165-169.

[31] K. Nagalakshmi, Avireni Srinivasulu, Cristian Ravariu, V. Vijay, V. V. Krishna, "A novel simple schmitt trigger circuit using CDTA and its application as a square-triangular waveform generator," J. Mod. Technol. Eng, vol. 3, 2018, pp. 205-216.

[32] Vallabhuni Vijay, C. V. Sai Kumar Reddy, Veerastu Sivanagaraju, Chandrashaker Pittala, "System for Minimizing Crosstalk Effects of Shells and Designing Multiwalled Carbon Nanotube Models," The Patent Office Journal No. 43/2019, India. International classification: B82Y10/00. Application No. 201941042460 A.

[33] V. Vijay, and Avireni Srinivasulu, "A DCCII Based Square Wave Generator With Grounded Capacitor," in proceedings of the 2016 IEEE International Conference on Circuits, Power and Computing Technologies (IEEE ICCPCT-2016), Kumaracoil, India, March 18-19, 2016, pp. 1–4.

[34] Krishna, VVS Vijay, A. Monisha, Sk Sadulla, and J. Prathiba, "Design and implementation of an automatic beverages vending machine and its performance evaluation using Xilinx ISE and Cadence," In 2013 Fourth International Conference on Computing, Communications and Networking Technologies (ICCCNT), IEEE, 2013, pp. 1–6.

[35] Vallabhuni Vijay, C. V. Sai Kumar Reddy, Chandrashaker Pittala, P ASHOK BABU, "System to Obtain Finite Gain and Noise of an Electrocardiogram Amplifier," The Patent Office Journal No. 43/2019, India. International classification: H03F3/38. Application No. 201941042674 A.

[36] Rajeev Ratna Vallabhuni, P Shruthi, G Kavya, S Siri Chandana, "6Transistor SRAM Cell designed using 18nm FinFET Technology," 2020 3rd International Conference on Intelligent Sustainable Systems (ICISS), Palladam, India, 2020, pp. 1584-1589.

[37] Shaik, Sadulla, and Prathiba Jonnala, "Performance evaluation of different SRAM topologies using 180, 90 and 45 nm technology,"In 2013 International Conference on Renewable Energy and Sustainable Energy (ICRESE), pp. 15-20. IEEE, 2013.

[38] Rajeev Ratna Vallabhuni, A. Karthik, CH. V. Sai Kumar, B. Varun, P. Veerendra, and Srisailam Nayak, "Comparative Analysis of 8-Bit Manchester Carry Chain Adder Using FinFET at 18nm Technology," 2020 3rd International Conference on Intelligent Sustainable Systems (ICISS), Palladam, India, December 4-5, 2020, pp. 1579-1583.

[39] Manchala Sreeja, Vallabhuni Vijay, "A Unique Approach To Provide Security For Women By Using Smart Device," European Journal of Molecular & Clinical Medicine, vol. 7, iss. 1, 2020, pp. 3669-3683.

[40] V. Vijay, and Avireni Srinivasulu, "Grounded Resistor and Capacitor based Square Wave Generator using CMOS DCCII," in proceedings of the 2016 IEEE International Conference

on Inventive Computation Technologies (IEEE ICICT-2016), Coimbatore, India, August 26-27, 2016, pp. 79–82.

[41] V. Siva Nagaraju, P. Ashok Babu, Vallabhuni Rajeev Ratna, Ramya Mariserla, “Design and Implementation of Low Power 32-bit Comparator,” Proceedings of the International Conference on IoT Based Control Networks and Intelligent Systems (ICICNIS 2020), Palai, India, December 10-11, 2020, pp. 1-8.

[42] B.M.S Rani, Divyasree Mikkili, Rajeev Ratna Vallabhuni, Chandra Shaker Pittala, Vijay Vallabhuni, Suneetha Bobbillapati, H. Bhavani Naga Prasanna, “Retinal Vascular Disease Detection from Retinal Fundus Images Using Machine Learning,” Australia patent 2020101450.

[43] Venkateswarlu, S.C., Kumar, N.U., Kumar, N.S., Karthik, A., and Vijay, V., “Implementation of Area optimized Low power Multiplication and Accumulation,” International Journal of Innovative Technology and Exploring Engineering (IJITEE), vol. 9, iss. 9, 2019, pp. 2278–3075.

[44] Vallabhuni Rajeev Ratna, M. Saritha, Saipreethi. N, V. Vijay, P. Chandra Shaker, M. Divya, Shaik Sadulla, “High Speed Energy Efficient Multiplier Using 20nm FinFET Technology,” Proceedings of the International Conference on IoT Based Control Networks and Intelligent Systems (ICICNIS 2020), Palai, India, December 10-11, 2020, pp. 1-8.

[45] Vallabhuni Vijay, C. V. Sai Kumar Reddy, Chandrashaker Pittala, Sonagiri China Venkateswarlu “System for Reducing Crosstalk Delays In Electronic Devices Using A CMOS Inverter,” The Patent Office Journal No. 43/2019, India. International classification: H03B5/18. Application No. 201941042515 A.

[46] Ratna, Vallabhuni Rajeev and M, Saritha and N, Saipreethi and V, Vijay and Shaker, P. Chandra and M, Divya and Sadulla, Shaik, High Speed Energy Efficient Multiplier Using 20nm FinFET Technology (January 19, 2021). ICICNIS 2020, Available at SSRN: https://ssrn.com/abstract=3769235 or http://dx.doi.org/10.2139/ssrn.3769235

[47] Vallabhuni Vijay, Pittala Chandra shekar, Shaik Sadulla, Putta Manoja, Rallabhandy Abhinaya, Merugu rachana, Nakka nikhil, “Design and performance evaluation of energy efficient 8-bit ALU at ultra low supply voltages using FinFET with 20nm Technology,” VLSI Architecture for Signal, Speech, and Image Processing, edited by Durgesh Nandan, Basant Kumar Mohanty, Sanjeev Kumar, Rajeev Kumar Arya, CRC press, 2021.

[48] Rajeev Ratna Vallabhuni, Jujavarapu Sravana, Chandra Shaker Pittala, Mikkili Divya, B.M.S.Rani, Vallabhuni Vijay, “Universal Shift Register Designed at Low Supply Voltages in 20nm FinFET Using Multiplexer,” Lecture Notes in Networks and Systems, 2021.

[49] V, Siva Nagaraju and P, Ashok Babu and Ratna, Vallabhuni Rajeev and Mariserla, Ramya, Design and Implementation of Low Power 32-bit Comparator (January 20, 2021). ICICNIS 2020, Available at SSRN: https://ssrn.com/abstract=3769748 or http://dx.doi.org/10.2139/ssrn.3769748

[50] Babu, P. Ashok, et al. "Realization of 8 x 4 Barrel shifter with 4-bit binary to Gray converter using FinFET for Low Power Digital Applications." Journal of Physics: Conference Series. Vol. 1714. No. 1. IOP Publishing, 2021.