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Power Efficient Shift Register Using Leakage Control NMOS Transistor

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Abstract- VLSI is a stream of electronics engineering thatoccupy putting millions and billions of transistors logically together on to a single chip. VLSI circuits play a vital role in modern digitalized world. FLIP-FLOPS (FFs) are the main storage elements utilized in digital system propose, that constitutes registers, shift registers, counters etc. The current utilization of the FFs employed in a typical digital design has a great influence on its performance. This paperpresentsthe design of a SISO (Serial In Serial Out) register using LCNT(Leakage Control NMOS Transistor) based D Flip Flop. The functional verification is done in mentor graphics tool. The obtained results matching with the expected ones and the comparative analysis with the previous design techniques shows that thiswill be an effective solution for the future low power register designs.

Keyword: LCNT, SISO

1. INTRODUCTION

In today's electronics planet, there is a drastic change in the size of devices. This led to the development of VLSI technology. It allows as design of circuitswith less power, portability and mobility, with less cost and less environmental effects. FLIP-FLOPS (FFs) are the main storage elements in digital system designs and they find applications in registers, shift registers, counter etc. The 20% - 45% of the total system power is from these basic storage elements. Therefore while designing registers, counters etc. the current utilization of a flip flop is the major performance limiting constraint. In a classic design model the major limitation of flip flops in VLSI designs is power consumption, current utilization, delay, clock skew etc. On concern with limitation current utilization is one of the significant constraints which reduce the speed of the device, reliability etc. Our motive is to decrease the current utilization using different low power methods. Using these flip flops we would like to design shift registers.

Shift registers are widely used in large number of sequential circuits and processors for temporary Limit of data. A development register is course from guaranteeing flip flop, bestowing a similar clock, done which those yield about each flip lemon will be related with data from asserting next flip lemon On chain. Sequential Previously, sequential out (SISO) development register recognizes data sequentially; specific case spot without a moment's delay In the lone enter line, Furthermore proceeded onward next flip flop sequentially. The yield will be additionally excelled a solitary yield transport for an equivalent sequential style.

Now-a-days, with the increasing use of mobile devices, laptops, consumer electronics demand a stringent constraint on reducing current utilization. Flip flops are the magic components utilized within successive advanced frameworks. Flip flops Furthermore latches are the essential components for those accumulate data. Flip flop is one of the most power utilization components. Flip flop can be implemented in different ways. Lector and LCNT techniques increase the efficiency of the design. Using Lector and LCNT the main attention has to decrease current utilization and increase the performance. There are two

types of D flip flops that are originate in literature that is single edge triggered and double edge triggered. But the double edge triggered Flip flop suffers from performance degradation, because it samples data on both clock edges. These single edge triggered Flip flops are simple in design and sample data only one clock edge. These are mostly designed by using master slave configuration. The limitation of conventional D flip flop based 4 bit SISO register is its performance characteristics such as current utilization, efficiency etc. This project presents design of 4 bit SISO using LCNT technique in order to overcome the limitation of conventional design.

2. SHIFT REGISTERS

The Shift Register is a sort of successive logic circuit that can be utilized for the capacity or the exchange of parallel information. Move Register is a route of flip flops, contains a related clock, wherein the output of every flip lemon is associated by the data involvement of the subsequent flip flop, resulting in a circuit that shifts by one place(as revealed in figure1 and 2) .

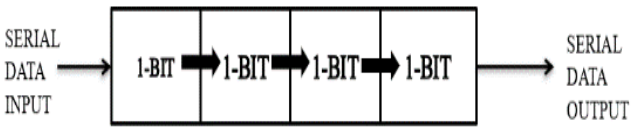

Figure1: Data transfer from left to right using shift register

CLOCK	T0	T1	T2	T3	T4	T5	T6	T7
SERIAL INPUT	1	0	1	1				
Q1		1	0	1	1			
Q2			1	0	1	1		
Q3				1	0	1	1	
Q4					1	0	1	1

Figure 2: Operation of 4-Bit SISO Shift Register

2.1 4-Bit Shift Registers using Conventional D-Flip Flop

The schematic of 4-bit shift registers using conventional D-flip flop is as revealed in figure 3 where conventional D-Flip Flops are connected in cascaded form with one input and one clock.

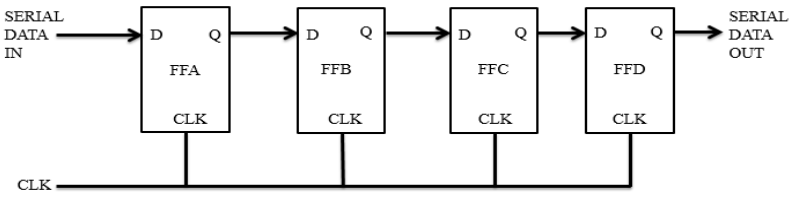

Figure 3: Schematic of 4-Bit Shift Registers Using Conventional D-Flip Flop

2.2 execution of Conventional D Flip Flop

In conventional D flip flop there are two clock signals one is positive clock and other is negative clock. There are pull up and pull down networks. The conventional D flip flop is plannedby means of master and slave networks. The yield of the master is specified to the slave as input, and also the output of the master is directly connected to the slave output. The main intention is to minimizing the current utilization. The logic diagram is as shown.

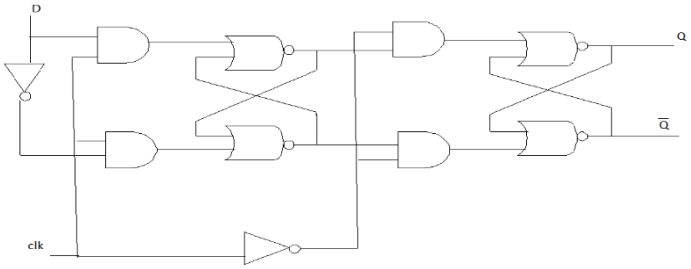

Figure 4: Conventional D-Flip Flop

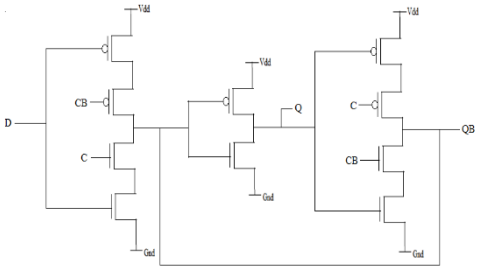

Figure 5: Schematic conventional D-Flip Flop

The conventional D flip flop circuit utilizes the double gated clock for both master and slave portions of the circuit. The hardware of gated checks gives supplements of master and slave. At the point when the output stays same despite the fact that the input or clock changes current is utilized regardless of the output was steady and do not alter.

2.3 Lector based D-Flip Flop

Lector is a strategy to diminish the issue of leakage in CMOS circuits; it incorporates two added leakage power transistors that are moderate, in the pathway from gracefully to ground which offers the additional opposition which will decrease the issue of escape present in the CMOS circuit. The lector actualized circuits have less power utilization when contrasted with regular circuit structure. When contrasted with regular circuit, lector strategy gives low static power dissemination. The Schematic of Lector based D flip failure is appeared in fig 6.

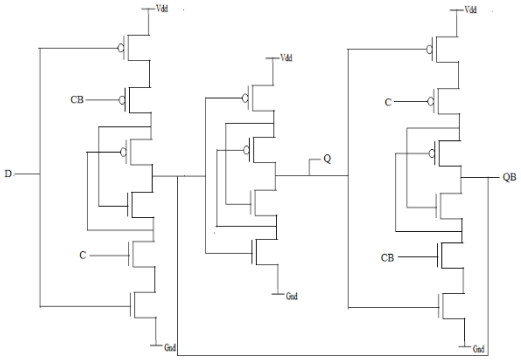

Figure 6: Schematic of Lector Based D-Flip Flop

3. PROPOSED 4-BIT SHIFT REGISTERS USING LCNT BASED D-FLIP FLOP

While comparing different design move towards for the D flip flop LCNT based design provide improved efficiency in conditions of supremacy dissipation. LCNT is a novel transistor level methodology for minimising of spillage power. This strategy actualizes, two LCTs inside a standard CMOS logic circuit. The LCNT Based circuits minimize the leakage power. The LCNT based D flip flop is revealed in fig 7.

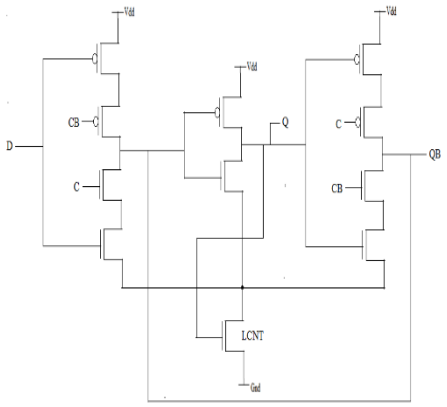

Figure 7: Schematic of LCNT Based D-Flip Flop

At the point when the LCNT is utilized in the circuit, just the inverter of the circuit gets influenced and the remainder of the circuit stays unaltered. After the progressions the authority dissemination gets decreased. The main contrast between the lector and LCNT is that is use n-channel MOSFET's, that give an expanded way opposition and lessen the current moving throughout it and consequently decreasing the power addicted.The projected 4 bit shift register using LCNT based flip flop is revealed in fig 8.

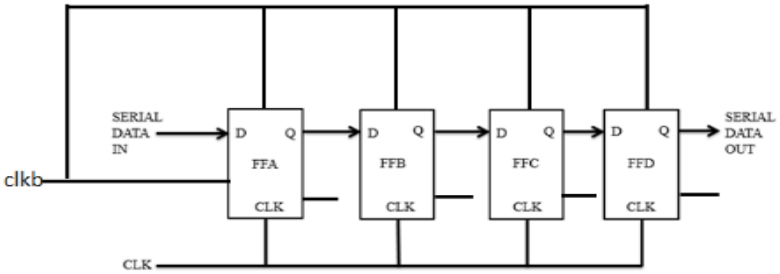

Figure 8:Block Diagram of 4-Bit Shift Registers Using LCNT Based D-Flip Flop

4. Results and Discussions

The designs are implemented using widely used X Manager EDA tools. The simulation and functional verifications are done with the help of Mentor Graphics 130nm technology. The schematic of 4 bit SISO register using conventional D flip flop and its output waveforms are revealed in fig 9 and 10.

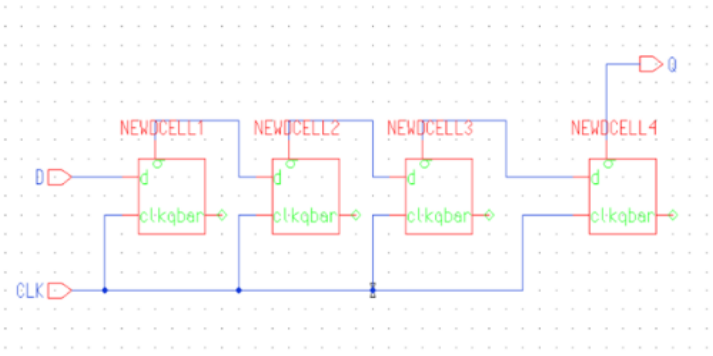

Figure9: Schematic of 4-bit conventional D flip flop

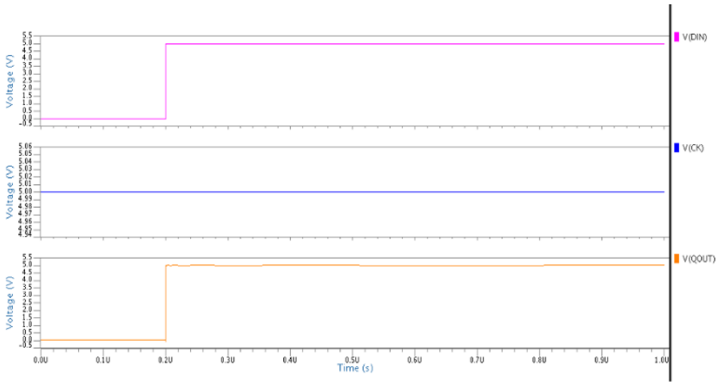

Figure10: Simulation waveforms of 4-bit conventional D-flip flop

The schematic and Simulation waveforms Of 4-Bit SISO using lector depended D flip flop is revealed in figure 11 and 12.

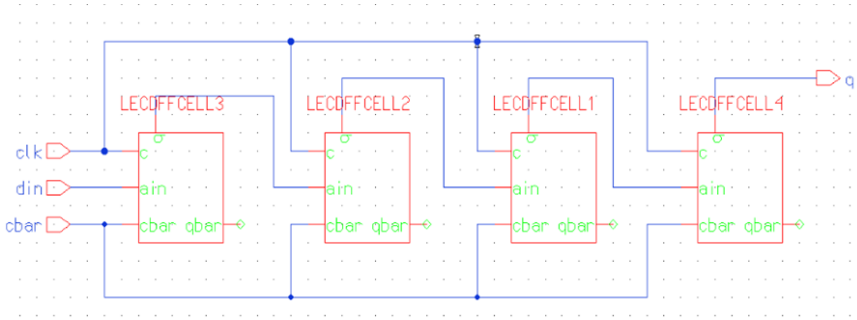

Figure.11: Schematic of 4-bit lector depended D flip flop

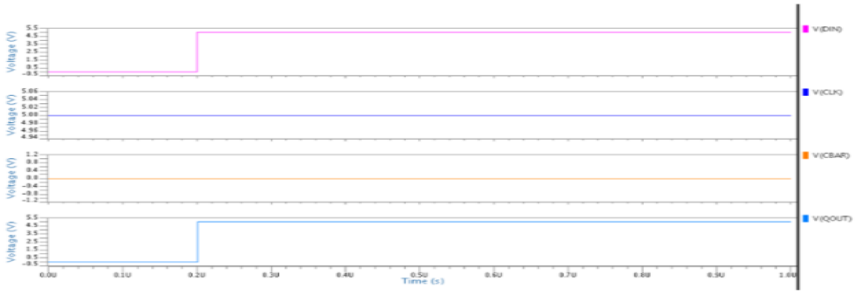

Figure.12: Simulation waveforms of 4-bit using lector based D-flip flop

The schematic and Simulation waveforms Of 4-Bit SISO using LCNT is revealed in figure 13 and 14

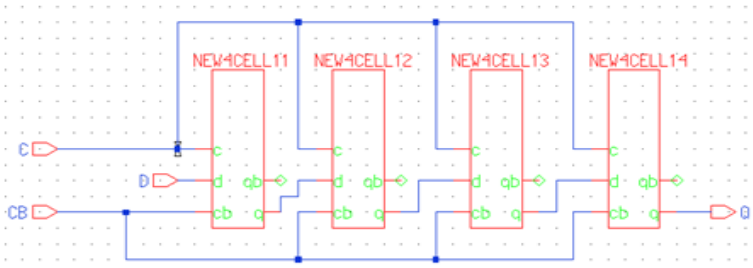

Figure.13: Schematic of 4-bit lcnt based D flip flop

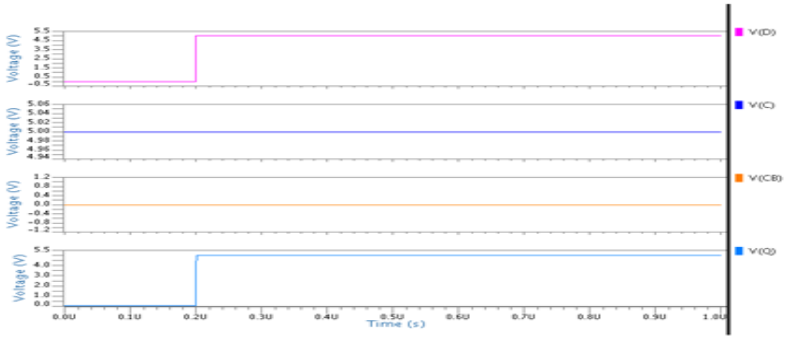

Figure.14: Simulation waveforms of 4-bit LCNT based D-flip flop

The comparative analysis of 4-bit SISO register using conventional, lector and LCNT based D flip flops is revealed in table1 in conditions of power and delay.

Techniques	Power Dissipation	Delay
Conventional D flip flop	21.4906nW	379.32ps
Lector based D flip flop	14.4500nW	854.98ps
Lcnt based D flip flop	10.4710nW	736.60ps

Table 1: Comparison of 4-bit SISO using different techniques

5. Conclusion

Flip flops are defined as the main building blocks of shift registers, counters, storage elements etc. While designing all these current utilization of flip flop is a major performance deciding factor. LCNT (Leakage control NMOS transistors) technique when applying to the flip flop can greatly reduce its effective current utilization. The paper presents an efficient implementation of 4-bit SISO register using LCNT based D flip flop with the help of mentor graphics 130nm technology. Further the design is compared with the SISO implemented using conventional as well as lector based flip flop.The simulation results as well the comparative analysis proves that LCNT based SISO register will be a proficient solution to the power efficient SISO register designs.

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