Design and Simulation of Heterogeneous Adder Using Xilinx Vivado

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Abstract
The adders are logic circuits designed to execute “high speed Arithmetic operations” in Arithmetic Logic Unit (ALU) utilized in processors. The basic Adders are “Half Adder and Full adder”. The diverse kinds of adders are Carry Look ahead Adder (CLA), Ripple Carry Adder (RCA), Carry Select Adder (CSLA), & Carry Skip Adder (CSKA). In this manuscript, Heterogeneous adder (HA) architecture is designed with support of diverse Homogeneous adders and Heterogeneous adders are contrasted with Homogeneous adders in terms of power, delay, & area. This architecture is based on a VHDL and compares their performance with Xilinx VIVADO software tool.
Keywords-Adders, RCA, CLA, Simulation, VHDL, Arithmetic Logic Unit (ALU), and Half Adder (HA), Full adder (FA)

1. Introduction
The arithmetic operations perform a significant role in numerous digital systems. The adders are the main modules in Digital signal Processors & Microprocessors. Adders have utilized to execute the Addition of numbers, Multiplication, Subtraction and Division operations. They require low efficient power and area designed technique to increment presentation of circuit. Hence, the area efficient design createsssmaller chip size and decreases the price. The dissimilar adders are RCA, CLA, CSLA, & CSKA.
Here Heterogeneous adder means concatenation of different homogeneous adders and Homogeneous adder is the combination of the same type of adders. The designed adder will be contrasted with each other in terms of power & area along with implementation & experimental results utilizing Xilinx VIVADO.

2. Related Work
A. Ripple Carry Adder
The RCA might be designed by “cascading full adder” in series i.e., carry from past FA will be connected as input carry for next phase. The FA will be an elementary building block of RCA. Hence, to design n-bit parallel adder, it needs n full adders. The block diagram of RCA will be shown in below figure.

![Fig.1: 4-Bit RCA](image_url)
Example: A=1010; B=0101; Cin =0 are the inputs of the adder than the output is S=1111 with a carry ‘0’.

The main restriction of RCA will be that as the delay & length of bit goes on enhances. Since every FA should wait for carry bit from previous FA. So RCA is relatively slow.

**B. Carry Look Ahead Adder**

The CLA is also identified as Fastest Adder. It develops speed by decreasing the amount of time needed to describe the carry bits. The flow diagram of CLA is displayed below:

The CLA estimates one or more carry bits before the sum that decreases wait time to estimate outcome of larger value bits. The CLA working might be understood by “Boolean expressions” dealing with FA and it will be provided by

- Carry propagate\((Pi)\) = A xor B
- Carry Generate\((Gi)\) = A and B

Both produce and propagate signals based only on input signals, the novel expressions for output sum and carry are

- Sum\((Si)\)= Pi xorCi \\
- Carryout\((Ci+1)=Gi+ Pi Ci

The limitation in CLA is if the bit length goes on increasing the circuit complexity is also increased.

**C. Carry Select Adder**

The CSLA comprises of multiplexer& 2RCAs. It comprises of an independent generation of sum and carry Cin=0 &Cin=1 have calculated parallel. On the basis of the Cin&external multipliers select the carry to next phase. Moreover, on the basis of carry input the sum is chooses, therefore, the delay will be decreased. The flow diagram of the CSLA will be shown in below figure.
D. Carry Skip Adder

The CSKA will be also identified as carry Bypass adder and that enhances on RCA delay. The enhancement of worst delay will be attained by utilizing numerous CSKAs to create a block skip adder.

The skip logic comprises of 1 multiplexer &m-input AND-gate. As propagate signals have contrasted in parallel and available early, the difficult way for skip logic in CSKA comprises only of delay imposed by multiplexer. The flow diagram of CSKA is displayed in below figure.

3. PROPOSED MODEL

The architecture of heterogeneous adder (HA) is suggested &designed with support of diverse architecture of homogeneous adder.

The proposed technique is 16-bit HA and it is concatenation of 8-bit RCA, 8-bit CLA. It will be compared with the 16-bit Homogeneous adder in terms of delay, area, &power. The flow diagram of 16-bit HA is represented in below figure.
4. RESULTS
1. Experimental Result for Proposed Method
2. 

![Experimental outcomes of suggested HA](image)

Fig.6: Experimental outcomes of suggested HA

3. Schematic Diagram for Proposed Method
4. 

![Schematic Diagram for suggested HA](image)

Fig.7: Schematic Diagram for suggested HA
5. Comparison and Tabulation

<table>
<thead>
<tr>
<th></th>
<th>8-Bit RCA</th>
<th>8-Bit CLA</th>
<th>Heterogeneous Adder</th>
<th>Homogeneous Adder</th>
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<tbody>
<tr>
<td>Slice LUTs</td>
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<td>17</td>
<td>25</td>
<td>38</td>
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<tr>
<td>Bonded IOB</td>
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<td>25</td>
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<td>0.02</td>
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<td>Utilization %(IO)</td>
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<td>8.67</td>
<td>14.67</td>
<td>16.67</td>
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</tbody>
</table>

Table 1: Comparison of Utilization among 8-Bit RCA, 8-Bit CLA, HA, Homogeneous Adder

<table>
<thead>
<tr>
<th></th>
<th>8-Bit RCA</th>
<th>8-Bit CLA</th>
<th>Heterogeneous Adder</th>
<th>Homogeneous Adder</th>
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</thead>
<tbody>
<tr>
<td>On-chip Memory</td>
<td>5.43w</td>
<td>5.60w</td>
<td>11.07w</td>
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<tr>
<td>Junction Temperature</td>
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<td>50.3°C</td>
<td>53.6°C</td>
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<tr>
<td>Thermal Margin</td>
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<td>43.7°C</td>
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<td>Signal (Data)</td>
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<td>0.17w</td>
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<td>0.367w</td>
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<td>0.083w</td>
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<tr>
<td>I/O</td>
<td>5.76w</td>
<td>5.28w</td>
<td>10.98w</td>
<td>11.96w</td>
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</table>

Table 2: Comparison of Power Summary between 8-Bit RCA, 8-Bit CLA, HA, Homogeneous Adder
Fig. 8: Comparison graph of HA usage

Fig. 9: Comparison graph of power consumption in Heterogeneous Adders

Fig 11: Comparison graph of power consumption in homogeneous adder
6. Conclusion

This manuscript suggests the HA with the use of 8-Bit RCA & 8-Bit CLA and simulation as stated by its properties utilizing VHDL in VIVADO. This method has low thermal margin under consumption of power. It has minimum delay & area that prove to be simple answer in developing speed of adder circuit. The relevant usage & powersummary of suggested method 16-Bit HA & 16-Bit Homogeneous adder was compared with the use of Bar-Graph.

7. References


