AN EFFICIENT DENOISING HARDWARE ARCHITECTURE OF CSA-FIR FILTER FOR REAL TIME ECG SIGNALS

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Abstract

In the recent years there is a huge demand for reduction in size and power of portable devices used for monitoring critical signals such as ECG. The technical advancements in VLSI has created a huge impact on biomedical signal processing. VLSI circuits working at high speed can be designed in order to consume less area and power. Especially for ECG signal denoising, digital filters such as FIR and IIR are used in most of the applications. Finite Impulse Filters (FIR) is used widely compared to IIR filters because of their good stability and high order. In this paper, FIR filter with modified carry save adder-based MACarchitectureis introduced to carryout ECG signal denoising application. The input raw ECG signal collected from MIT-PhysionetArrhythmia data base is read using MATLAB and coefficients are generated. resource efficient FIR filter is designedby using carry save adder.Therefore, a carry save adder circuit can be invented with minimal area and power consumption. It is evident that the power line interference noise has been removed and denoised ECG signals have been obtained. And these noises have been removed from ECG MIT-BIH Arrhythmia database (record# 100,101,102 &103). It has 14.98 % less area, 8.83% lees power, 26.24% less delay, 22.48% less APP and 37.29% less ADP.

Key Words

Electrocardiogram, Very Large-Scale Integrated Circuit Design, Finite Impulse Response, Multiply Accumulate.

1. Introduction

Many studies have been done by researchers on ECG denoising.In recent Years, in most of the signal processing applications, FIR filter is used as a major building block.The type of filters that contain these elements allow us to obtain almost any form of digital signal. The N-length FIR filter is constructed with combinations of adders, multipliers and a series of delays to establish the sequence of the filter output. Computers have memory delays that only work on swappable samples and they use coefficients passed in to multiply the with the samples. The output is the sum of all the samples delayed multiplied by sufficient coefficients. Manually, most FIR filter implementations are undertaken in transposition direct form [1], [2], [3]. The multiplier is a key

part of a FIR network filter. In order to design a FIR filter, the MAC (Multiply and Accumulate) units are typically used.To perform the filter operation, the overall architecture of FIR filter requires more area as it contains more multipliers. So, for FIR filter design the most important task is to reduce the area of multipliers [4], [5], [6], [7], [8], [9], [10], [11].MAC units can be optimized for power and timing as proposed in[12]. For real time ECG signals, the FIR based MAC units are used to suppress the “Power Line Interference (PLI)” noise. The efficiency of a FIR filter depends on the speed of the MAC device.Various windowing methods for FIR filter such as Rectangular, Hanning, Kaiserand Blackman window have been proposed earlier [13]. At the expense of high computational load and as the order of the filter is large, Kaiser and rectangular window have shown better results. Among the various windowing methods discussed above, FIR Kaiser Window filter provides better performance [14]. But a FIR filter with MAC unit gives better performance in terms of power, area and speed [15].Digital filter implementations of FPGAs and other VLSI chips allow higher sampling rates and lower cost for processing media data than “Digital Signal Processing (DSP)” chips. Digital filters are used widely as they can achieve much better signal to noise ratio than analog filters.

2. Literature Review

Figure 1, represents an ECG waveform. ECG is an important functional indicator of the heart that is used to diagnose heart problems. It contains essential points such as P-Q-R-S-T. An ECG, which has five main components called "P" "Q" "R" "S" "T" and the range of frequencies for a patient who is ambulatory is 0.5 Hz to 50 Hz [16]. On an EKG the first and last cardiac cycles are indicative of a single step in blood flow of the heart. The QRS complex is the largest amplitude portion of the electrocardiogram since it is caused by the depolarization of cell [17].

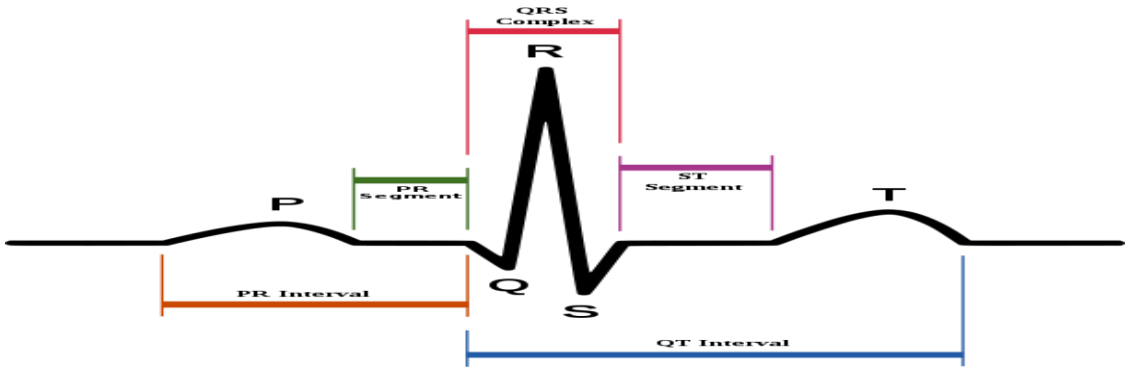

Fig. 1: Pictorial representation for ECG signal waveform of normal heart beat

There are different forms of noises that interfere with the ECG signal. Both ECG signal noises can be easily produced from the interference of the ECG signal itself or due to biological discharges or electric discharges [13], [18]. Considerable attention was paid to various denoising techniques.Filter design that enables power line interference removal is discussed here[19]. This paper concentrates on an Efficient Denoising Hardware Architecture for Real time ECG signals.

Efficient architecture of FIR filter is most effective for ECG signal denoising. Several methods on FIR architectures which had proposed in last ten years has been discussed in this section. It presents some of the important works on FIR filter architectures with their pros and cons.

Author	Method	Merits	Demerits
Park and Meher [20]	In order to minimize sampling time and complexity of area, new pipeline architecture is used and fast bit clock for signed carry -saving accumulation.	It is greatly enhanced by updating of the LUT and implementation of filtering and weight-updating algorithms.	For most operations, there should be a fast bit clock but for very short PIO products, a slower bit clock is to be used.
Jiajia Chen et al. [21]	This is a new algorithm to synthesize coefficients of finite precision with low Implementation costs from the linear phase FIR filter's frequency response requirements.	The principle of sensitivity to under expression and the margin of frequency response error was added.	Design is implemented by using MATLAB only. hardware complexity and speed parameters are not discussed.
Durgesh Nandan et al. [22]	Proposed new algorithm and hardware design for logarithm multiplier for FIR filter.	It is greatly enhanced by reducing the hardware complexity of logarithm multiplier and FIR filter.	It is a type of approximate multiplier. Not suitable for exact applications.
M. Sumalatha et al. [23]	FIR filtering is applied to the ECG data signal, the Vedic architecture Carry Lookahead Adder is implemented.	The signal is used to calculate the "Mean Square Error (MSE)", "Bit Error Rate (BER)" and "Noise Ratio Signal (SNR)" Output.	Design mainly focuses on multiplier optimization.
Y. Arpitha et al. [24]	FIR filter with modified Vedic multiplier-based architecture is introduced to carry out ECG signal denoising application.	Hardware efficient design of vedic multiplier is developed in FIR filter for ECG signal denoising	Design mainly focusses on multiplier optimization.
R. Rohini [1]	Literature review of existing FIR filter presented	Summarizes works already completed in the area of FIR filter design.	hardware architecture of FIR filter is not discussed here.

FPGA based adaptive filter have been proposed to remove the power line interference noise in [1].In this paper architecture for FIR filter have been developed and implemented using Spartan board and "Xilinx system generator (XSG)" software to eliminate the power line interference noise.

3. Problem Statement

The study discusses the performance of the various available filtering systems, methodologies, merits, and demerits in the literature review section. The researchers are currently working on creating a module for denotations of ECG signals on a regular basis. In the section of this paper stated, a focus is laid on the limits of the FIR filter. In addition to the proposed design theory of this new filter, the researchers pointed out how the architecture itself addresses the shortcomings of current FIR literature-based filters. The following are issues with the FIR filtering architecture.

1) Adder is one of the area consuming components in FIR filter. If adder architectureis hardware efficient then FIR filter architecture becomes efficient.

2) Efficient pipeline process also plays important role to make FIR filter hardware efficient.

Solutions: “Seamless Distribution dependent carrying (SPDEB)”, using “Carry Save Adder (CSA)” [25], can be used for the creation of hardware-saving FIR filter architectures in the overcoming these limitations of FIR filter design. Seamless pipelining technique is used for equal treatment of components regarding component optimization. As a result of thispipelining, reduced delays are obtained. The specification of the ECG denoising application is carried outusing CSA-FIR system.

4. Carry save adder-FIR filter methodology

Figure 2 represents the overall block diagram for ECG signal denoising. ECG signal is first from standard data base and add some noise is added and then it is converted into binary form. Then it is converted into text format and applied to the CSA-FIR filter. FIR filter output was translated and read signals via MATLAB into text format. Finally, the ECG signal was denoised and several parameters such as SNR, BER, MSE can be measured. We have the Effective hardware efficient CSA-FIR filter is proposed here. Finally Seamless pipelining is used to reduce the proposed FIR filter's delay. FIR Filter's hardware-effective architecture is very commonly used to denoise the ECG signal.

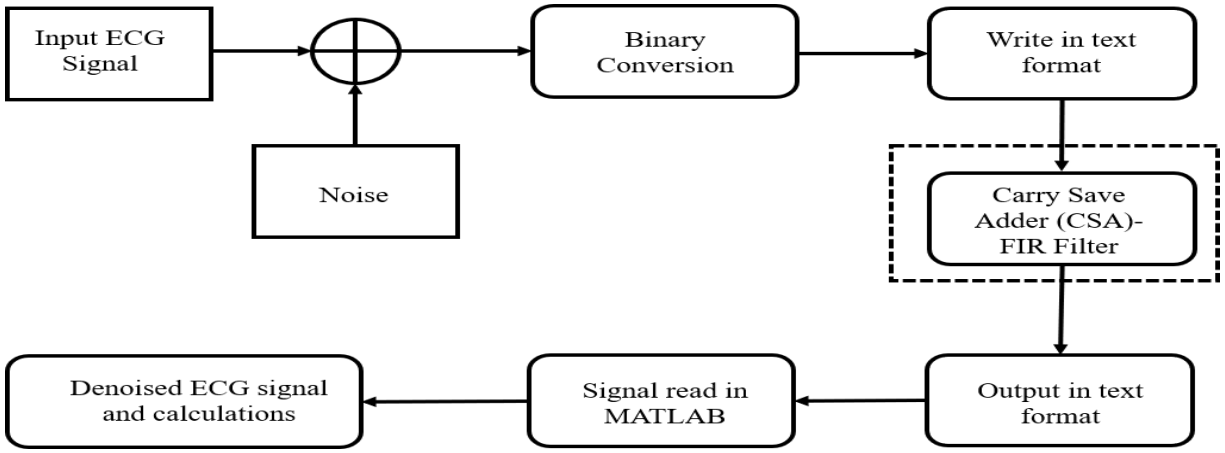

Fig 2. Overall Block diagram of ECG signal denoising

4.1 Carry save adder-based FIR filter architecture

The block diagram of carry save adder-based FIR filter architecture is shown in Fig 3 consists of multiplier, carry save adders and delay units.

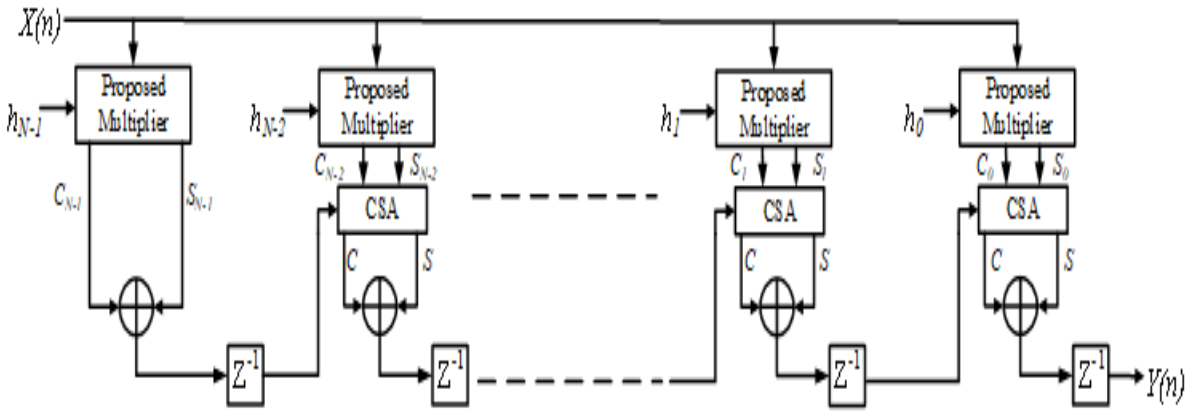

Fig 3. Proposed architecture of FIR filter by using CSA

The common form of N-tap programmable FIR filter is given below in equation (1).

$$y(n) = \sum_{k=1}^{N-1} h(\mathrm{k})x(n-k) \qquad (1)$$

Here n=0, 1, 2…etc, y (n) is represented as the output of the FIR filter, h (k) is the coefficient of FIR filter. x (n-K) is represented as the number of the input sequence. General architecture of programmable FIR filter has been shown in Figure 4.

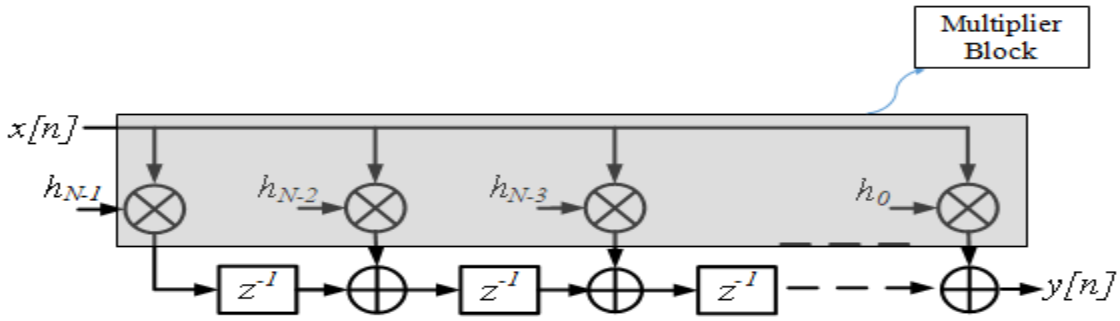

Fig 4. Programmable FIR filter basic Architecture

5. Experimental Results and Discussion

In this section, the proposed method and the obtained experimental results are discussed along with the performance measures. The performance of the proposed method is evaluated using MATLAB and ASIC 180 nm technology. The proposed is implemented using 8 GB RAM, I7 8th generation and 2 TB hard disk. For verification purpose coding was done in Verilog. The input raw ECG signal collected from MIT-PhysionetArrhythmia data base is read using MATLAB and coefficients are generated. Synopsys design compiler 180 nm technology is used for area, power and delay analysis.

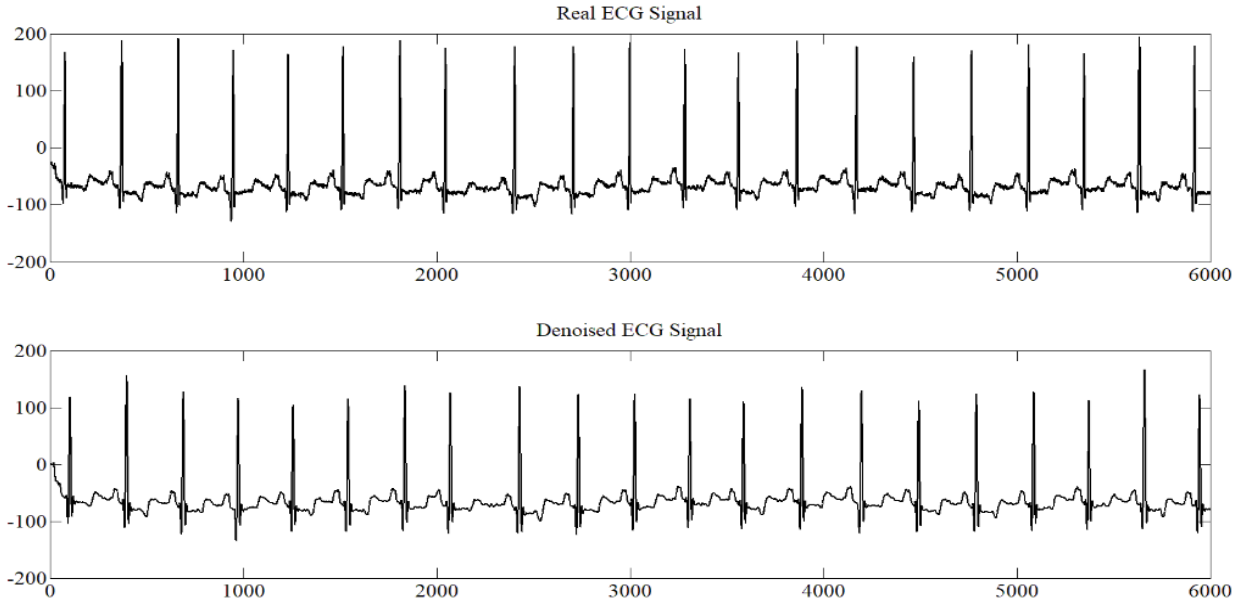

Fig 5. MATLAB generated graph of real ECG signal and denoised ECG signal for Input signal sample 100

Denoising is performed for Input signal-100 sample, Input signal-101 sample, Input signal-102 sample and Input signal-103 sample. Figure 5 showsGraph of real ECG signal and denoised ECG signal for Input signal sample 100 by using proposed FIR filter.

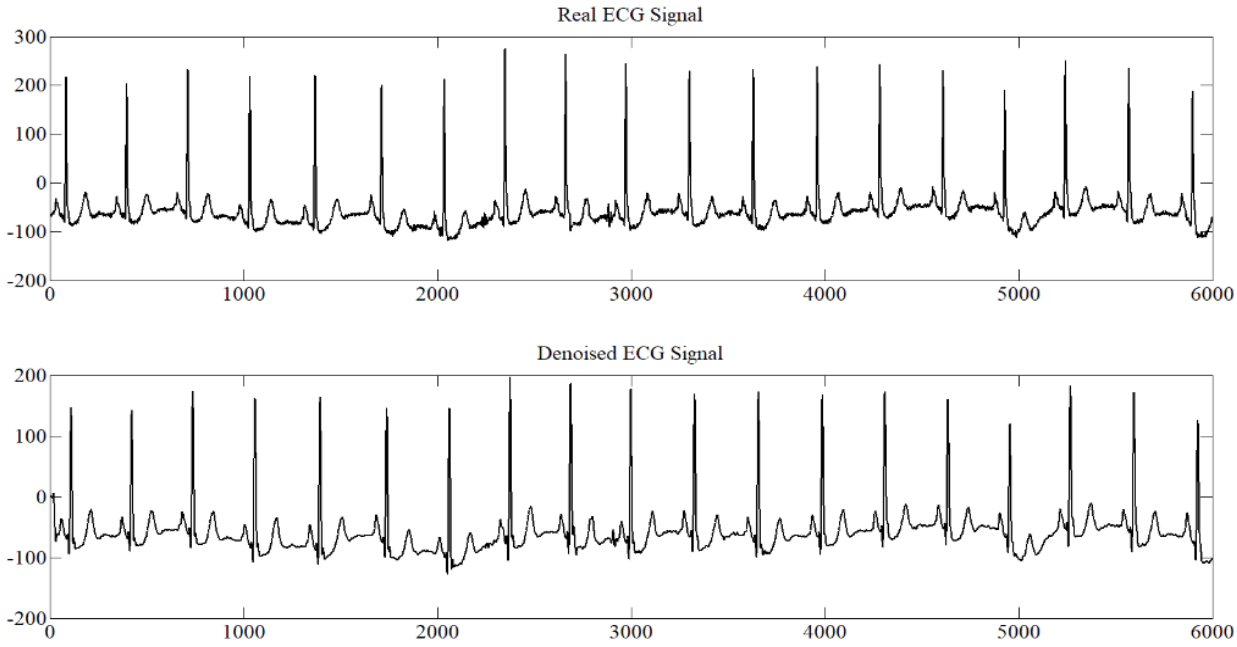

Fig 6. Shows graph of real ECG signal and denoised ECG signal for Input signal sample 101

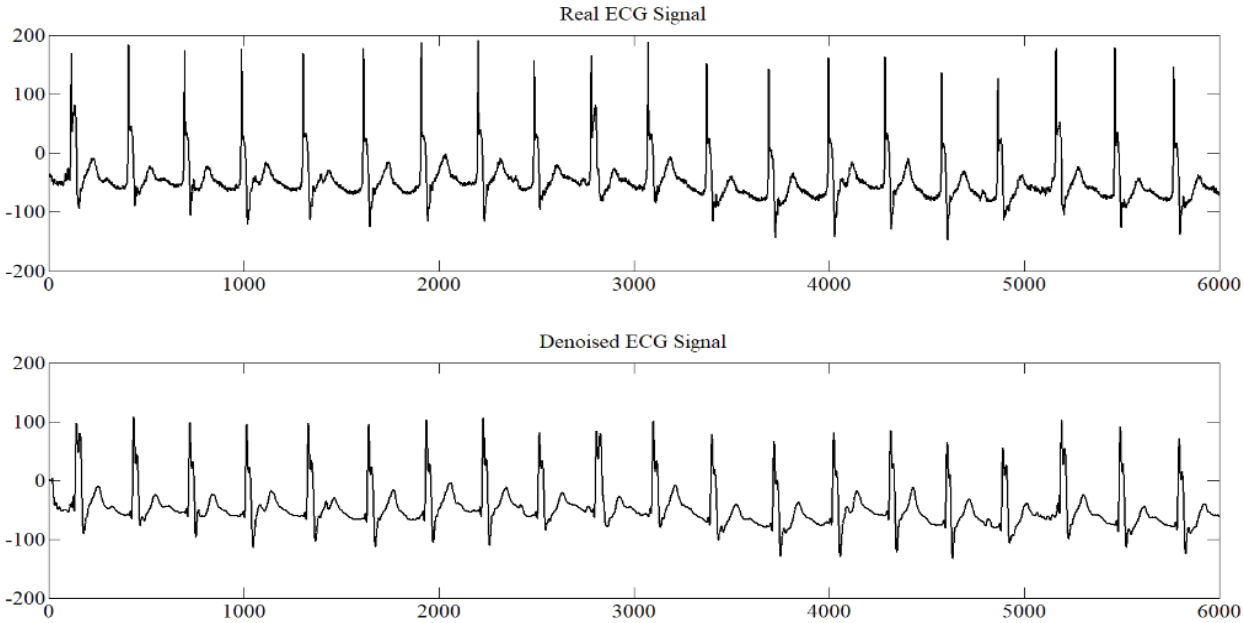

Fig 7. Shows graph of real ECG signal and denoised ECG signal for Input signal sample 102

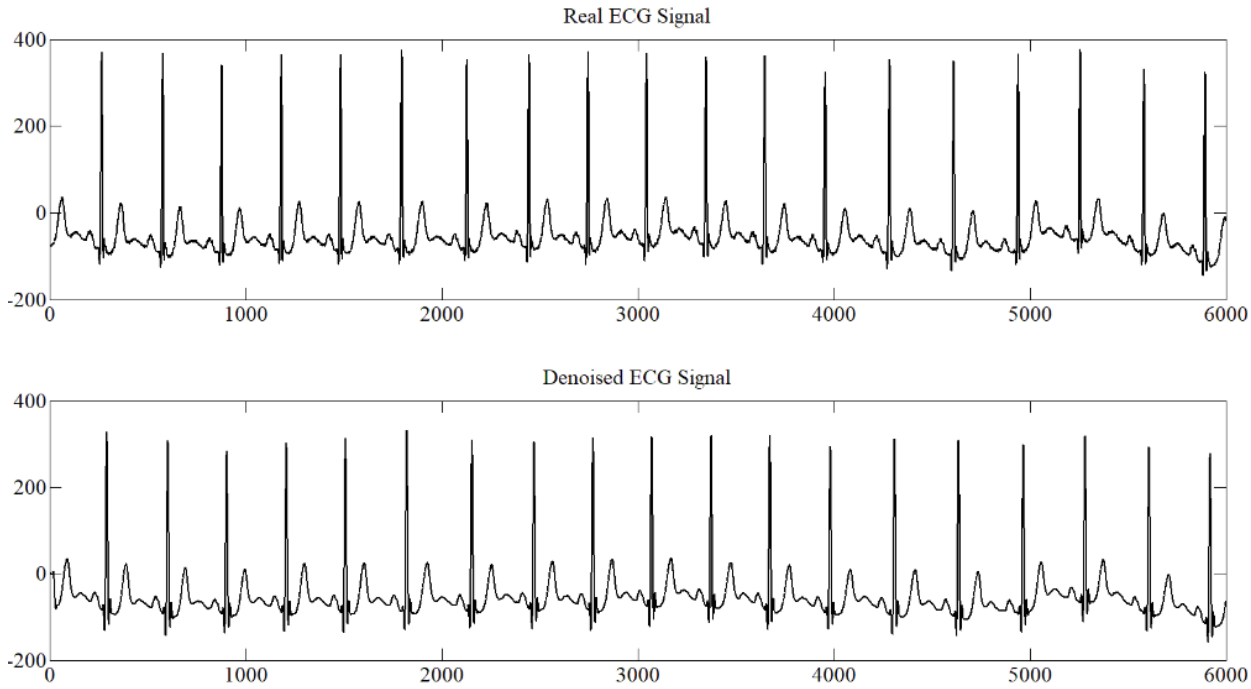

Fig 8. Shows graph of real ECG signal and denoised ECG signal for Input signal sample 103

Figure 6,7 and 8 shows generated graphs of real ECG signal and denoised ECG signal for Input signal sample 101 by using proposed FIR filter, Input signal sample 102 and Input signal sample 103. The databases related to noisy ECG signals have been taken from Physionet.org and MIT-BIH Arrhythmia (record 100,101,102& 103) have been selected. Filter coefficients are generated using MATLAB. The filter specifications have been taken as cutoff frequency is 50Hz, stop band attenuation is 50dB, pass band attenuation is 0.1dB, Normalized pass band frequency is 0.1*pi, Normalized stop band frequency is 0.2*pi and sampling frequency is chosen as 500Hz

The table 1 represents the comparison of the conventional 8 Tap FIR filter architecture and the proposed 8 Tap CSA-FIR filter architecture. The outputs of both the methods are tabulated in Table 1. The output of the proposed method is mainly focused on reduction of hardware utilization. For conventional FIR filter 287302 μm^2, 47.93 mW and 12.88 ns are required but in the proposed FIR filter utilizes only 244264 μm^2, 43.70 mW and 09.5 ns. Regarding Area power product (APP) conventional design takes 13770384.9 um^2*mW and proposed design takes 10674336.8 um^2*mW. Regarding Area Delay product (ADP) then conventional design takes 3700449.76 μm^2*ns and proposed design takes 2320508 um^2*mW. Table 2 shows percentage reduction of the ASIC performance for the CSA-FIR filter method in comparison with the conventional FIR filter.Proposed 8 Tap FIR filter is proved to have efficient hardware architecture. It has 14.98 % less area, 8.83% lees power, 26.24% less delay, 22.48% less APP and 37.29% less ADP.

Table 1. Experimental Results of ASIC performance for existing and CSA-FIR filter method

Technology	Method	Length	Area (μm^2)	Power (mW)	Delay (ns)	APP (um^2*mW)	ADP (μm^2*ns)
180 nm Technology	Conventional FIR	8 Tap	287302	47.93	12.88	13770384.9	3700449.76
	Proposed FIR	8 Tap	244264	43.70	9.5	10674336.8	2320508

Table 2. Reduction percentage of the ASIC performance for the CSA-FIR filter method

Technology	Length	Reduction of Area (%)	Reduction of Power (%)	Reduction of Delay (%)	Reduction of APP (%)	Reduction of ADP (%)
180 nm Technology	8 Tap	14.98	8.83	26.24	22.48	37.29

Conclusion

With the proposed method, it is evident that the power line interference noise has been removed and denoised ECG signals have been obtained. And these noises have been removed from ECG MIT-BIH Arrhythmia database (record# 100,101,102 &103). The obtained denoised waveforms for the four ECG records have been shown above.Proposed 8 Tap FIR filter shows efficient hardware architecture. It has 14.98 % less area, 8.83% lees power, 26.24% less delay, 22.48% less APP and 37.29% less ADP.

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